AiP2206
Bidirectional I^2C-busand SMBus Voltage-level Translator

Product Specification

Specification Revision History：

Version	Date	Description
2022-02-A1	2022-02	New

Contents

1、General Description

AiP2206 is a bidirectional I^2C-bus and SMBus voltage-level translator with an enable port and is operational from 1.0V to 3.6V($V_{ref(1)}$)and 1.8V to 5.5V($V_{bias(ref)(2)}$).

AiP2206 allows bidirectional voltage-level translation from 1V to 5V without the use of direction pins. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. When the enable port is high, the translator switch is on, and SCL1 and SDA1 are connected to SCL2 and SDA2 respectively, allowing data transmission at both ends. When the enable port is low, the switch is off and the ports are high-impedance state.

AiP2206 will isolate both sides when the device is disabled, and provides voltage-level translation when enabled.

AiP2206 can be used to run two buses, one is at 400kHz operating frequency and the other is at 100kHz operating frequency. If these two buses are at different frequencies, the 100kHz bus must be isolated when the other bus is operating at 400kHz. If the controller runs at 400kHz, the maximum system operating frequency may be lower than 400kHz due to the delay of the translation.

Like the standard I2C system, AiP2206 needs to provide logic high level for translation bus through pull-up resistor. AiP2206 has a standard I^2C bus open-collector configuration. The pull-up resistance is determined by the transmission rate of the system, but both ends of the translator must have pull-up resistors. This device mainly works in I^2C bus devices of standard mode, fast mode and fast mode Plus to cooperate with SMBus devices. The maximum frequency depends on the RC time constant, but it is generally allowed more than 2MHz.When the SDA1 or SDA2 port is low level, it is ON-state between SDA1 and SDA2 and there is a small ON-state resistor. Assuming that the reference high level of the device at SDA2 is higher than the reference high level of the device at SDA1, the output voltage at SDA1 will be limited to the voltage set by VREF1 when the device at SDA2 outputs a high level. When the device at SDA1 outputs a high level, SDA2 is pulled up by pull-up resistor to the high level set by the drain pull-up power supply voltage ($V_{pu(D)}$). This allows users to freely switch high and low levels without direction control pins. The operating principle of SCL1/SCL2 channel is the same as that of SDA1/SDA2 channel.

All the channels have the same electrical characteristics, and there is a slight deviation in voltage or propagation delay from one side to the other. Symmetric manufacturing of switches is beneficial to solve the voltage-level translation of split transistors. The translator provides excellent ESD protection for low-voltage devices, and at the same time, it protects devices lacking electrostatic protection.

Features:

- Standard mode, fast mode and fast mode plus I^2C-bus and SMBus compatible
- Less than1.5ns maximum propagation delay to accommodate standard mode and fast mode I^2C-bus devices and multiple controllers
- Allows voltage-level translation between:
  1.0V $V_{ref(1)}$ and 1.8V，2.5V，3.3V or 5V $V_{bias(ref)(2)}$
  1.2V $V_{ref(1)}$ and 1.8V，2.5V，3.3V or 5V $V_{bias(ref)(2)}$
  1.8V $V_{ref(1)}$ and 3.3V or 5V $V_{bias(ref)(2)}$
  2.5V $V_{ref(1)}$ and 5V $V_{bias(ref)(2)}$
  3.3V $V_{ref(1)}$ and 5V $V_{bias(ref)(2)}$
- Provides bidirectional voltage-level translation with no controlling pins

- Low 3.5Ω ON-state resistor is routed between input and output ports and provides less signal distortion
- Open-drain I^2C bus I/O port (SCL1，SDA1，SCL2 and SDA2)
- 5V tolerant I^2C bus I/O port, to allow mixed mode signal operation
- High-impedance state of SCL1, SDA1, SCL2 and SDA2EN ports when EN is low-level
- Lock-up free operation
- Package form: TSSOP8

Ordering Information:

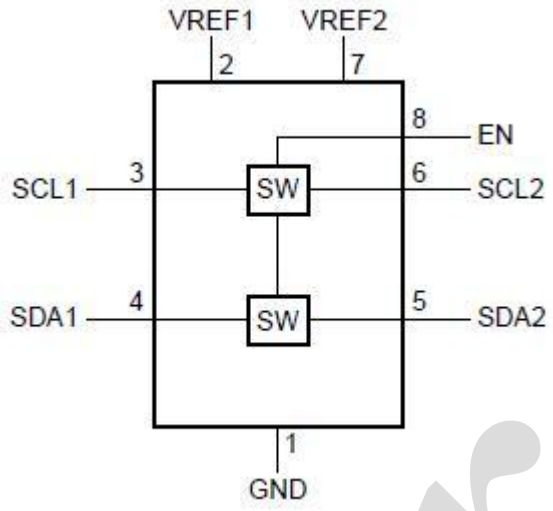
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP2206TA8.TR	TSSOP8	2206	6000PCS/reel	6000PCS/box	Size of plastic enclosure: 3.0mm×3.0mm Pin spacing: 0.65mm

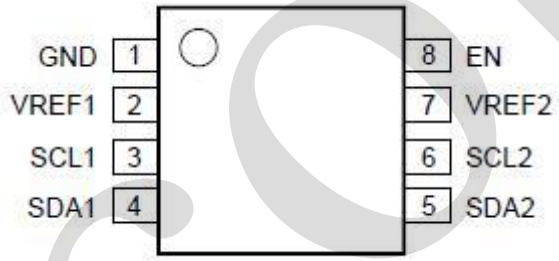
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	GND	Ground
2	VREF1	Low-voltage side, reference voltage of SCL1 and SDA1
3	SCL1	Serial clock, low-voltage side, routed to VREF1 through a pull-up resistor
4	SDA1	Serial data, low-voltage side, routed to VREF1 through a pull-up resistor
5	SDA2	Serial data, high-voltage side, routed to VREF2 through a pull-up resistor
6	SCL2	Serial data, high-voltage side, routed to VREF2 through a pull-up resistor
7	VREF2	High-voltage side, reference voltage of SCL2 and SDA2
8	EN	Enable switch input, routed to VREF2 and a high pull-up resistor

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, unless otherwise specified)

Characteristic	Symbol	Conditions	Value	Unit
reference voltage	$V_{ref(1)}$	-	-0.5 to 9	V
reference bias voltage	$V_{bias(ref)(2)}$	-	-0.5 to 6	V
input voltage	V_I	-	-0.5 to 6	V
input/output pin voltage	$V_{I/O}$	-	-0.5 to 6	V
channel current	I_{ch}	-	0 to 128	mA
input clamp current	I_{ik}	V_I<0V	-50 to 0	mA
storage temperature	T_{stg}	-	-65 to 150	℃
soldering temperature	T_L	10s	250	℃

3.2、Recommended Operating Conditions

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
input/output pin voltage	$V_{I/O}$	SCL1, SDA1, SCL2, SDA2	0	-	5	V
reference voltage	$V_{ref(1)}$	VREF1	0	-	5	V
reference bias voltage	$V_{bias(ref)(2)}$	VREF2	0	-	5	V
enable input	$V_{I(EN)}$	-	0	-	5	V
ON-state current	$I_{sw(pass)}$	-	-	-	64	mA
ambient temperature	T_{amb}	-	-40	-	85	℃

Note: $V_{ref(1)} \leq V_{bias(ref)(2)} - 1V$ for best results in voltage-level translation.

3.3、Electrical Characteristics

3.3.1、DC Characteristics

(T_{amb}=-40 to 85℃, unless otherwise specified)

Characteristic	Symbol	Conditions		Min.	Typ.	Max.	Unit
input clamp voltage	V_{IK}	I_I=−18mA; $V_{I(EN)}$=0V		-	-	-1.2	V
High-level input current	I_{IH}	V_I=5V; $V_{I(EN)}$=0V		-	-	5	uA
ON Resistance	R_{ON}	SCLn，SDAn；V_I=0V；I_O=64mA	$V_{I(EN)}$=4.5V	-	2.4	5	Ω
			$V_{I(EN)}$=3V	-	3	6	Ω
			$V_{I(EN)}$=2.3V	-	3.8	8	Ω
			$V_{I(EN)}$=1.5V	-	15	32	Ω
		V_I=2.4V；I_O=15mA	$V_{I(EN)}$=4.5V	-	4.8	7.5	Ω
			$V_{I(EN)}$=3V	-	46	80	Ω
		V_I=1.7V；I_O=15mA	$V_{I(EN)}$=2.3V	-	40	80	Ω

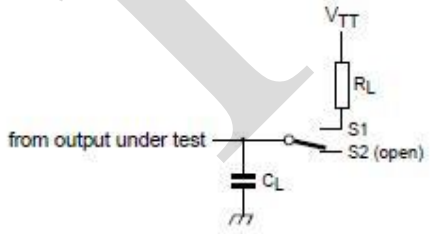
Note: All typical values are at T_{amb}=25℃.

3.3.2、AC Characteristics

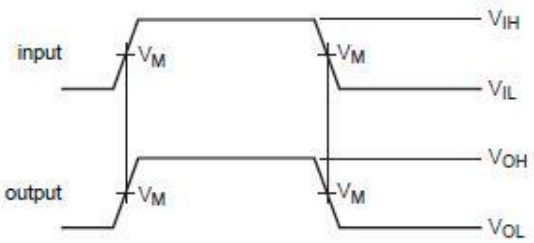
(T_{amb}=-40 to 85℃, unless otherwise specified)

Parameter	Symbol	Conditions	C_L=50pF		C_L=30pF		C_L=15pF		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Low to High propagation delay	t_{PLH}	$V_{I(EN)}$=3.3V; V_{IH}=3.3V; V_{IL}=0V; V_M=1.15V, from(input)SCL2 or SDA2 to (output)SCL1 or SDA1	0	2	0	1.2	0	0.6	ns
High to Low propagation delay	t_{PHL}		0	2	0	1.5	0	0.75	ns
Low to High propagation delay	t_{PLH}	$V_{I(EN)}$=2.5V; V_{IH}=2.5V; V_{IL}=0V; V_M=0.75V, from(input)SCL2 or SDA2 to (output)SCL1 or SDA1	0	2	0	1.2	0	0.6	ns
High to Low propagation delay	t_{PHL}		0	2.5	0	1.5	0	0.75	ns
Low to High propagation delay	t_{PLH}	$V_{I(EN)}$=3.3V; V_{IH}=2.3V; V_{IL}=0V; V_{TT}=3.3V; V_M=1.15V; R_L=300, from(input)SCL1 or SDA1 to (output)SCL2 or SDA2	0	1.75	0	1	0	0.5	ns
High to Low propagation delay	t_{PHL}		0	2.75	0	1.65	0	0.8	ns
Low to High propagation delay	t_{PLH}	$V_{I(EN)}$=2.5V; V_{IH}=1.5V; V_{IL}=0V; V_{TT}=2.5V; V_M=0.75V; R_L=300Ω, from(input)SCL1 or SDA1 to (output)SCL2 or SDA2	0	1.75	0	1	0	0.5	ns
High to Low propagation delay	t_{PHL}		0	3.3	0	2	0	1	ns

Load circuit for outputs



Load circuit



Timing diagram

Note: C_L includes jig capacitor. All input pulses supplied by generators have the following characteristics: P_{RR}≤10MHz； Z_o=50Ω； t_r≤2ns； t_f≤2ns。

4、Function Description

4.1、Bidirectional Translation

For bidirectional clamp configuration, the EN port must be connected to VREF2 and both ports need to be connected to $V_{pu(D)}$ through a typical pull-up resistor of 200 KΩ. This will allow VREF2 to control EN port. It is recommended to add a filter capacitor on VREF2. The master output of I^2C bus can be push-pull output or open-drain output (pull-up resistor required); and the device output of I^2C bus can be push-pull output or open-drain output (SCL2 and SDA2 need pull-up resistor to be connected to $V_{pu(D)}$). However, if any output is a push-pull output, the data must be unidirectional or the output must be a three-state gate controlled by some direction-control mechanism to prevent high-to-low level competition in any direction. If the outputs are both open-drain outputs, direction control will not be necessary.

The supplied reference voltage ($V_{ref(1)}$) is connected to the power supply voltage of controller. When $V_{ref(2)}$ is connected to the power supply voltage ($V_{pu(D)}$) of 3.3V～5.5V through a 200kΩ resistor, and $V_{ref(1)}$ is set between 1V and ($V_{pu(D)}$-1V), SCL1 and SDA1 can output a voltage equal to VREF1 at the maximum, and SCL2 and SDA2 can output a voltage equal to $V_{pu\,(d)}$ at the maximum.

4.2、How to Seize Pull-up Resistor Value

The pull-up resistor of open-drain bus is determined by different application schemes, and is also dependent on the following driving characteristics:

- Driving current
- The driver of V_{OL}
- The driver of V_{IL}
- Operating frequency

The following table data can be used to evaluate the pull-up resistance of different application schemes, so as to determine the minimum pull-up resistance. Table 1, Table 2 and Table 3 contain the recommended minimum pull-up resistance of AiP2206 circuit under typical translation level and driving current. The resistance is calculated under the same specified driving current. V_{OL}=V_{IL}=0.1×V_{CC} (±5% tolerance of power supply voltage and ±1% tolerance of resistance). It should be noted that the resistor finally selected in the application scheme should be equal to or larger than the values in Table 1, Table 2 and Table 3. It can unsure that the transmitted low level is less than 10% of V_{CC} voltage, and the external driver should be able to obtain the sink current from the pull-up resistor. For GTL circuit, the resistance table should be recalculated to explain the bias voltage limit among ON-state resistance, $V_{CC(B)}$ and $V_{CC(A)}$.

A-side	B-side						Unit
	1.2V	1.5V	1.8V	2.5V	3.3V	5V	
1.0V	$R_{pu(A)}$=750 $R_{pu(B)}$=750	$R_{pu(A)}$= 845 $R_{pu(B)}$= 845	$R_{pu(A)}$= 976 $R_{pu(B)}$= 976	$R_{pu(A)}$=none $R_{pu(B)}$= 887	$R_{pu(A)}$=none $R_{pu(B)}$=1180	$R_{pu(A)}$=none $R_{pu(B)}$=1820	Ω
1.2V	-	$R_{pu(A)}$= 931 $R_{pu(B)}$= 931	$R_{pu(A)}$=1020 $R_{pu(B)}$=1020	$R_{pu(A)}$=none $R_{pu(B)}$ =887	$R_{pu(A)}$=none $R_{pu(B)}$=1180	$R_{pu(A)}$=none $R_{pu(B)}$=1820	Ω
1.5V	-	-	$R_{pu(A)}$=1100 $R_{pu(B)}$=1100	$R_{pu(A)}$=none $R_{pu(B)}$ =866	$R_{pu(A)}$=none $R_{pu(B)}$=1180	$R_{pu(A)}$=none $R_{pu(B)}$=1780	Ω
1.8V	-	-	-	$R_{pu(A)}$=1470 $R_{pu(B)}$=1470	$R_{pu(A)}$=none $R_{pu(B)}$= 150	$R_{pu(A)}$=none $R_{pu(B)}$=1780	Ω
2.5V	-	-	-	-	$R_{pu(A)}$=1960 $R_{pu(B)}$=1960	$R_{pu(A)}$=none $R_{pu(B)}$=1780	Ω
3.3V	-	-	-	-	-	$R_{pu(A)}$=none $R_{pu(B)}$=1740	Ω

Table 1 Pull-up Resistor Minimum Value, 3mA Sink Current Driver

A-side	B-side						Unit
	1.2V	1.5V	1.8V	2.5V	3.3V	5V	
1.0V	$R_{pu(A)}$ =221 $R_{pu(B)}$ =221	$R_{pu(A)}$ =225 $R_{pu(B)}$ =225	$R_{pu(A)}$ =287 $R_{pu(B)}$ =287	$R_{pu(A)}$=none $R_{pu(B)}$ =267	$R_{pu(A)}$=none $R_{pu(B)}$ =357	$R_{pu(A)}$=none $R_{pu(B)}$ =549	Ω
1.2V	-	$R_{pu(A)}$ =274 $R_{pu(B)}$ =274	$R_{pu(A)}$ =309 $R_{pu(B)}$ =309	$R_{pu(A)}$=none $R_{pu(B)}$ =267	$R_{pu(A)}$=none $R_{pu(B)}$ =357	$R_{pu(A)}$=none $R_{pu(B)}$ =549	Ω
1.5V	-	-	$R_{pu(A)}$ =332 $R_{pu(B)}$ =332	$R_{pu(A)}$=none $R_{pu(B)}$ =261	$R_{pu(A)}$=none $R_{pu(B)}$ =348	$R_{pu(A)}$=none $R_{pu(B)}$ =536	Ω
1.8V	-	-	-	$R_{pu(A)}$ =442 $R_{pu(B)}$ = 442	$R_{pu(A)}$=none $R_{pu(B)}$ =348	$R_{pu(A)}$=none $R_{pu(B)}$ =536	Ω
2.5V	-	-	-	-	$R_{pu(A)}$ =590 $R_{pu(B)}$ =590	$R_{pu(A)}$=none $R_{pu(B)}$ =523	Ω
3.3V	-	-	-	-	-	$R_{pu(A)}$=none $R_{pu(B)}$ =523	Ω

Table 2 Pull-up Resistor Minimum Value, 10mA Sink Current Driver

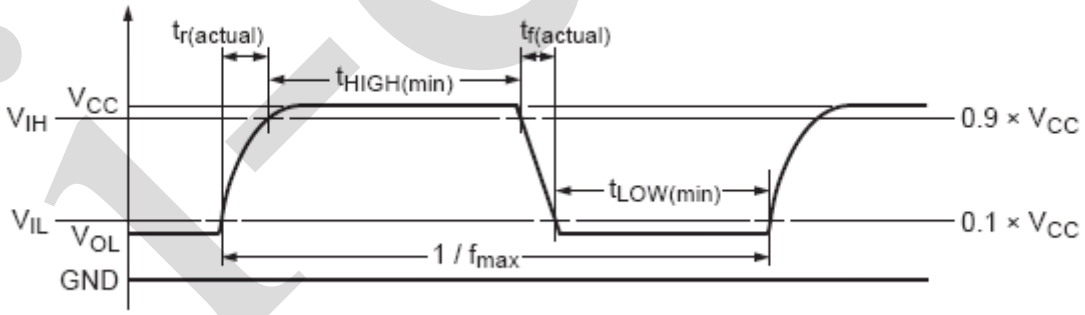
A-side	B-side						Unit
	1.2V	1.5V	1.8V	2.5V	3.3V	5V	
1.0V	$R_{pu(A)}$=147 $R_{pu(B)}$=147	$R_{pu(A)}$=169 $R_{pu(B)}$=169	$R_{pu(A)}$=191 $R_{pu(B)}$=191	$R_{pu(A)}$=none $R_{pu(B)}$=178	$R_{pu(A)}$=none $R_{pu(B)}$=237	$R_{pu(A)}$=none $R_{pu(B)}$=365	Ω
1.2V	-	$R_{pu(A)}$= 182 $R_{pu(B)}$= 182	$R_{pu(A)}$= 205 $R_{pu(B)}$= 205	$R_{pu(A)}$=none $R_{pu(B)}$= 178	$R_{pu(A)}$=none $R_{pu(B)}$=237	$R_{pu(A)}$=none $R_{pu(B)}$)=365	Ω
1.5V	-	-	$R_{pu(A)}$= 221 $R_{pu(B)}$= 221	$R_{pu(A)}$=none $R_{pu(B)}$=174	$R_{pu(A)}$=none $R_{pu(B)}$= 232	$R_{pu(A)}$=none $R_{pu(B)}$=357	Ω
1.8V	-	-	-	$R_{pu(A)}$=294 $R_{pu(B)}$=294	$R_{pu(A)}$=none $R_{pu(B)}$=232	$R_{pu(A)}$=none $R_{pu(B)}$=357	Ω
2.5V	-	-	-	-	$R_{pu(A)}$=392 $R_{pu(B)}$=392	$R_{pu(A)}$=none $R_{pu(B)}$=357	Ω
3.3V	-	-	-	-	-	$R_{pu(A)}$=none $R_{pu(B)}$=348	Ω

Table 3 Pull-up Resistor Minimum Value, 15mA Sink Current Driver

4.3、How to Design Maximum Operating Frequency

The maximum frequency is limited by voltage rising/falling time and minimum pulse width of high and low levels. The following formula is an example of maximum frequency calculation. The rising time and falling time are shown in the figure.

$$f_{max} = \frac{1}{t_{LOW(min)} + t_{HIGH(min)} + t_{r(actual)} + t_{f(actual)}}$$



The rising and falling edges depend on the translation level, driving strength, and total node capacitance ($C_{L(tot)}$) on the bus and the pull-up resistor (R_{pu}). Node capacitance is the sum of PCB wiring capacitance and device capacitance in the bus. Due to the influence of peripheral circuit, PCB layout and different operating conditions, the calculation of rising edge and falling edge is very complicated and there will be some inflection points on the curve.

The main component of rising edge and falling edge is RC time in bus. At this time, the circuit has two basic operating states: one is low impedance when the circuit is ON; the other is that port A and port B are isolated when the circuit is OFF.

The falling edge time, that is, the process of the output of An or Bn from high to low, is described as follows: the voltage of port B must be reduced to $V_{CC(A)}$ first no matter which port operates first . This time depends on the pull-up resistor, the driving strength of communication equipment and the capacitor. When the voltage drops below $V_{CC(A)}$, the channel resistance disappears so that port A and port B are equal. The capacitance of these two ports constitutes the total capacitance, and the pull-up resistors of these two ports are combined into parallel equivalent resistors. Compared with the pull-up resistor, R_{on} of the circuit is quite small, so its influence on the pull-up resistor can be neglected, and the falling process depends on the total capacitance and the driving current of the pull-up resistor. The estimation of the actually falling time in the circuit is equal to the time for B port to drop to $V_{CC(A)}$ plus the time for two ports to drop from $V_{CC(A)}$ to V_{IL}.

The rising edge time, that is, the process of An or Bn output from low to high, is described as follows (takes Bn output as an example). When the signal is low and R_{on} is the minimum, then port A and port B are essentially a node. They will rise together with a fixed RC time constant, which is the sum of all the capacitance and equivalent resistance of these two ports. When the signal is close to $V_{CC(A)}$ voltage, the channel resistance appears, the waveform is separated, and the voltage of B port will rise with RC time constant determined only by the peripheral environment of B port until the voltage stops changing. For An side, the process that the voltage rises to $V_{CC(A)}$ is essentially the same.

The following basic guidelines can help optimize the circuit operation:

● The path length is kept to a minimum value by keeping NVT circuit close to the processor.

● The round trip time of the signal on the path should be less than the rising or falling edge of the signal to reduce reflection.

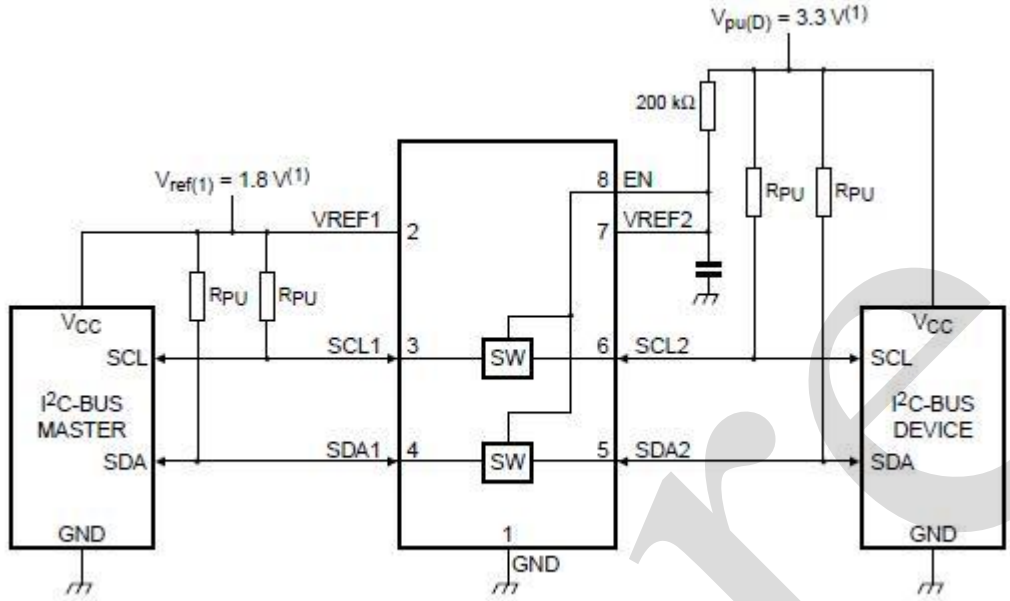
● The faster the rising and falling edge of the signal, the higher the chance of closed loop.

● The stronger the driving strength of the pull-up resistor (up to 15mA), the higher the operating frequency that the circuit can use.

The system designer must rely on the limitation of peripheral driving current and node capacitance (minimizing the length of wires, stubs, connectors and paths) to design the resistance of pull-up resistor to obtain the expected operating frequency.

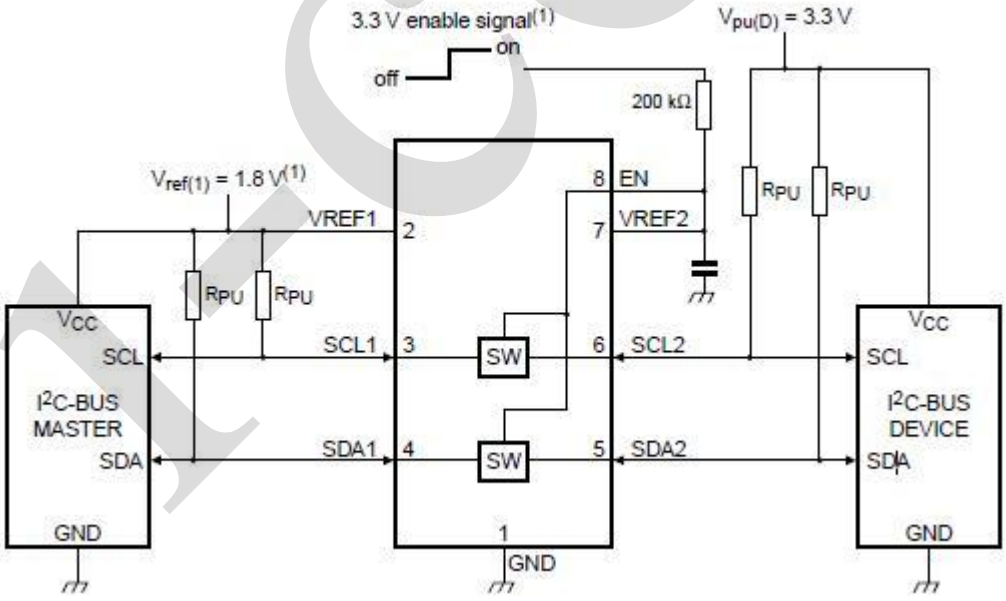
5、Typical Application Circuit And Application Note

5.1、Typical Application Circuit 1 (Switch is Always Enabled)



Note: It is suggested to make $V_{bias(ref)(2)}$ be at least 1V higher than $V_{ref(1)}$ when setting $V_{ref(1)}$ and $V_{pu(D)}$ so that for best translator operation.

5.2、Typical Application Circuit 2(Switch Enable Control)



Note: It is suggested to make Vbias(ref)(2) be at least 1V higher than Vref(1) when setting Vref(1) and Vpu(D) so that for best translator operation in enable mode.

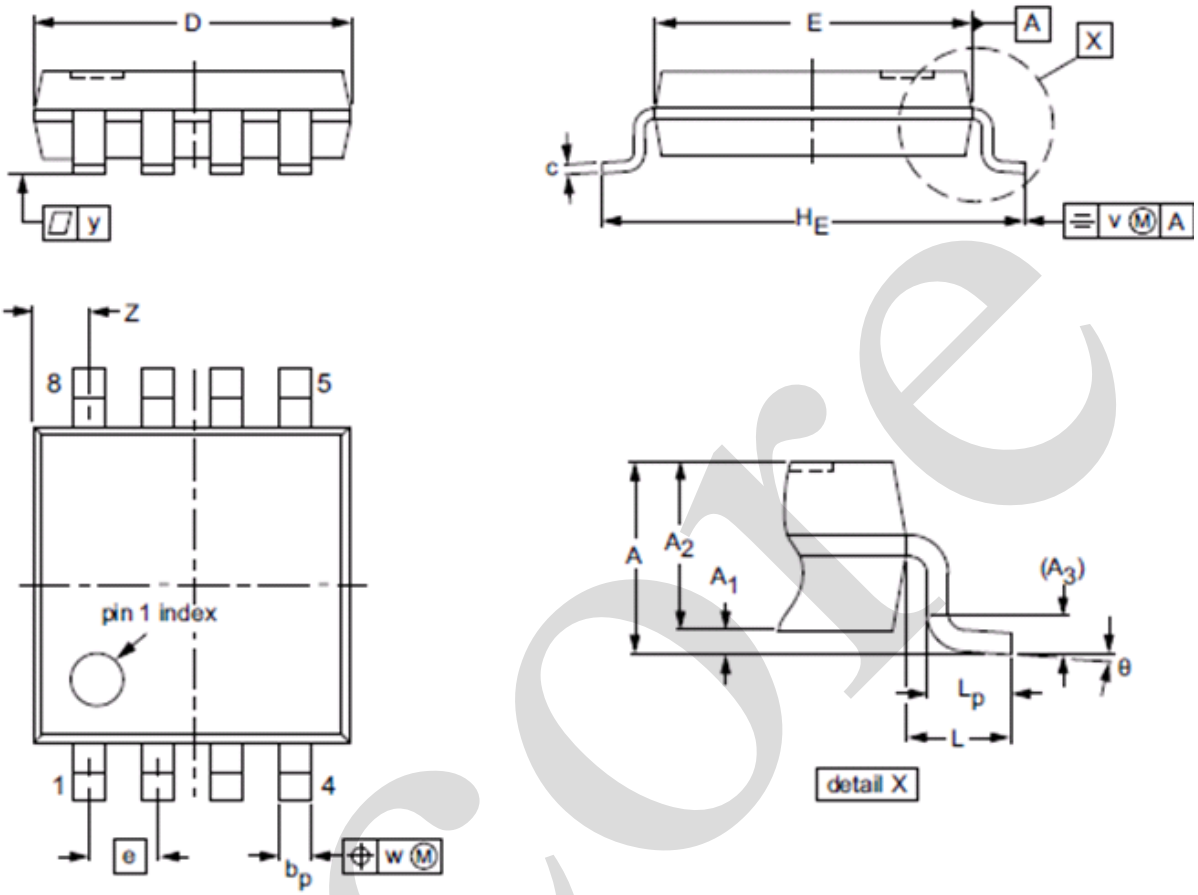
5.3、Application Operating Conditions

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
reference bias voltage	$V_{bias（ref）（2）}$	-	$V_{ref(1)}$ +0.6	2.1	5	V
EN input voltage	$V_{I（EN）}$	-	$V_{ref(1)}$ +0.6	2.1	5	V
reference voltage	$V_{ref（1）}$	-	0	1.5	4.4	V
pass switch current	$I_{sw（pass）}$	-	-	14	-	mA
reference current	I_{ref}	transistor	-	5	-	uA
ambient temperature	T_{amb}	-	-40	-	85	℃

Note: All typical values are at T_{amb}=25℃.

6、Package Information

6.1、TSSOP8



UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

Recommended carefully reading this information before the use of this product；

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