AiP74LVC/LVCH16373
16-bit D-type transparent latch; 3-state

Product Specification

Specification Revision History:

Version	Date	Description
2017-12-A1	2017-12	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The AiP74LVC/LVCH16373 are 16-bit D-type transparent latches featuring separate D-type inputs with bus hold (AiP74LVCH16373 only) for each latch and 3-state outputs for bus-oriented applications. One Latch Enable (LE) input and one Output Enable($\overline{OE}$) are provided for each octal. Inputs can be driven from either 3.3V or 5V devices.When disabled, up to 5.5V can be applied to the outputs. These features allow the use of these devices in mixed 3.3V and 5V applications.

The device consists of two sections of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition, the latches are transparent, that is, the latch outputs change each time its corresponding D-input changes. The latches store the information that was present at the D-inputs one set-up time (t_{su}) preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. Bus hold on the data inputs eliminates the need for external pull-up resistors to hold unused inputs.

Features:

- 5V tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range from 1.2V to 3.6V
- CMOS low power consumption
- Multibyte flow-through standard pinout architecture
- Multiple low inductance supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (AiP74LVCH16373 only)
- High-impedance when V_{CC}=0V
- Specified from -40℃ to +125℃
- Packaging information: TSSOP48

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVC16373 TA48.TB	TSSOP48	74LVC16373	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm
AiP74LVCH16373 TA48.TB	TSSOP48	74LVCH16373	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVC16373 TA48.TR	TSSOP48	74LVC16373	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm
AiP74LVCH16373 TA48.TR	TSSOP48	74LVCH16373	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

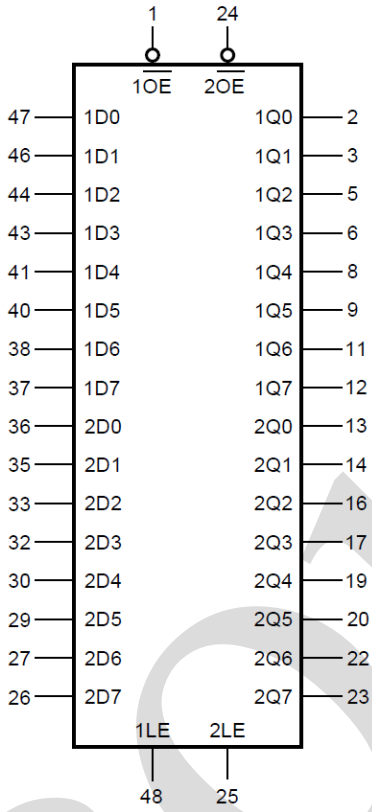


Figure 1. Logic symbol

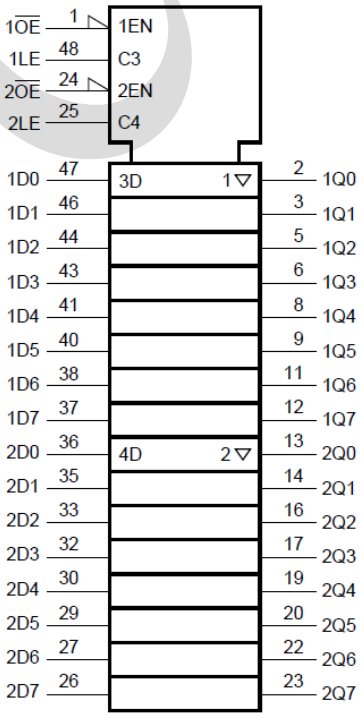


Figure 2. IEC logic symbol

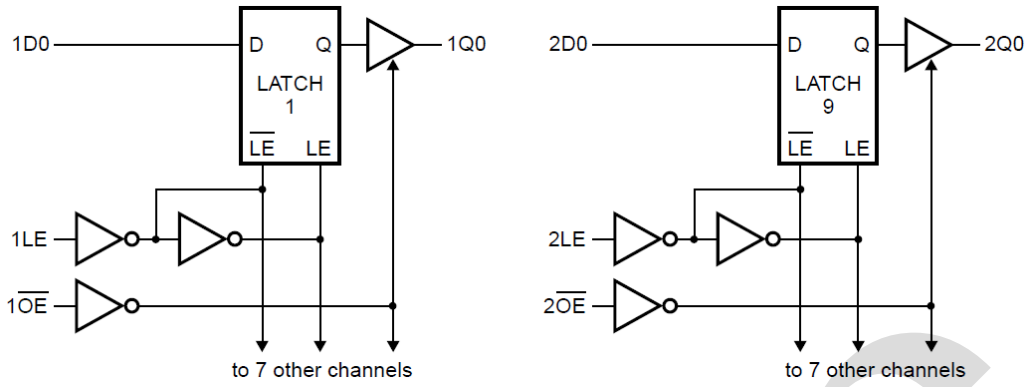


Figure 3. Logic diagram

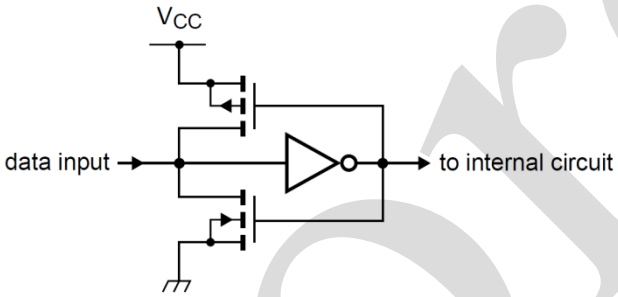
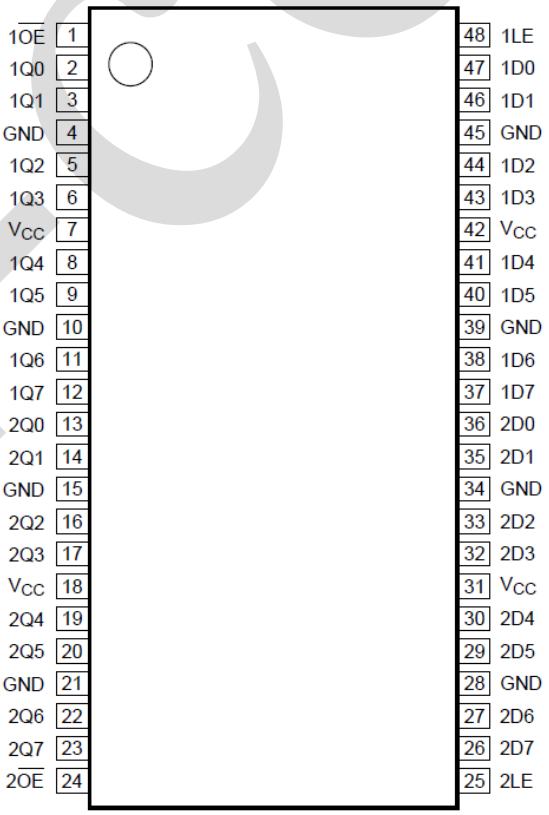


Figure 4. Bus hold circuit

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	$1\overline{OE}$	output enable input (active LOW)
24	$2\overline{OE}$	output enable input (active LOW)
48	1LE	latch enable input (active HIGH)
25	2LE	latch enable input (active HIGH)
4,10,15,21,28,34,39,45	GND	ground (0V)
7,18,31,42	V_{CC}	supply voltage
2,3,5,6,8,9,11,12	1Q0 to 1Q7	data output
13,14,16,17,19,20,22,23	2Q0 to 2Q7	data output
47,46,44,43,41,40,38,37	1D0 to 1D7	data input
36,35,33,32,30,29,27,26	2D0 to 2D7	data input

2.4、Function Table

Operating modes	Input			Internal latch	Output
	$n\overline{OE}$	nLE	nDn		nQ0 to nQ7
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Note:

H=HIGH voltage level

h=HIGH voltage level one set-up time prior to the HIGH to LOW LE transition

L=LOW voltage level

l=LOW voltage level one set-up time prior to the HIGH to LOW LE transition

Z=high-impedance OFF-state

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+6.5	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
input voltage	V_I	-[1]	-0.5	+6.5	V
output clamping current	I_{OK}	V_O>V_{CC} or V_O<0V	-	±50	mA
output voltage	V_O	output HIGH or LOW state[2]	-0.5	V_{CC}+0.5	V
		output 3-state[2]	-0.5	+6.5	V
output current	I_O	V_O=0V to V_{CC}	-	±50	mA
supply current	I_{CC}	-	-	100	mA
ground current	I_{GND}	-	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	260		℃

Note:

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	1.65	-	3.6	V
		functional	1.2	-	3.6	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃
input transition rise and fall rate	Δt/ΔV	V_{CC}=1.65V to 2.7V	0	-	20	ns/V
		V_{CC}=2.7V to 3.6V	0	-	10	ns/V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65×V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 3.6V	V_{CC}-0.2	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.2	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.8	-	-	V
			I_O=-12mA; V_{CC}=2.7V	2.2	-	-	
			I_O=-18mA; V_{CC}=3.0V	2.4	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.2	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 3.6V	-	-	0.2	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.45	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.6	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.4	V
			I_O=24mA; V_{CC}=3.0V	-	-	0.55	V
input leakage current	I_I	V_{CC}=3.6V; V_I=5.5V or GND[2]		-	-	±5	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL};V_{CC}=3.6V; V_O=5.5V or GND[2]		-	-	±5	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=5.5V		-	-	±10	uA
supply current	I_{CC}	V_{CC}=3.6V;V_I=V_{CC} or GND; I_O=0A		-	-	20	uA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=2.7V to 3.6V; V_I=V_{CC}-0.6V; I_O=0A		-	-	500	uA
input capacitance	C_I	V_{CC}=0V to 3.6V; V_I=GND to V_{CC}		-	5.0	-	pF
bus hold LOW current	I_{BHL}	V_{CC}=1.65V; V_I=0.58V[3][4]		10	-	-	uA
		V_{CC}=2.3V; V_I=0.7V		30	-	-	uA
		V_{CC}=3.0V; V_I=0.8V		75	-	-	uA
bus hold HIGH current	I_{BHH}	V_{CC}=1.65V; V_I=1.07V[3][4]		-10	-	-	uA
		V_{CC}=2.3V; V_I=1.7V		-30	-	-	uA
		V_{CC}=3.0V; V_I=2.0V		-75	-	-	uA
bus hold LOW	I_{BHLO}	V_{CC}=1.95V[3][5]		200	-	-	uA
		V_{CC}=2.7V		300	-	-	uA

overdrive current		V_{CC}=3.6V	500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	V_{CC}=1.95V[3][5]	-200	-	-	uA
		V_{CC}=2.7V	-300	-	-	uA
		V_{CC}=3.6V	-500	-	-	uA

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

[2] The bus hold circuit is switched off when V_I>V_{CC} allowing 5.5V on the input pin.

[3] Valid for data inputs (AiP74LVCH16373) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65×V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 3.6V	V_{CC}-0.3	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.05	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.65	-	-	V
			I_O=-12mA; V_{CC}=2.7V	2.05	-	-	
			I_O=-18mA; V_{CC}=3.0V	2.25	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.0	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 3.6V	-	-	0.3	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.65	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.8	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.6	V
			I_O=24mA; V_{CC}=3.0V	-	-	0.8	V
input leakage current	I_I	V_{CC}=3.6V; V_I=5.5V or GND[2]		-	-	±20	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL};V_{CC}=3.6V; V_O=5.5V or GND[2]		-	-	±20	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=5.5V		-	-	±20	uA
supply current	I_{CC}	V_{CC}=3.6V;V_I=V_{CC} or GND; I_O=0A		-	-	80	uA
additional	ΔI_{CC}	per input pin;		-	-	5000	uA

supply current		V_{CC}=2.7V to 3.6V; V_I=V_{CC}-0.6V; I_O=0A				
bus hold LOW current	I_{BHL}	V_{CC}=1.65V; V_I=0.58V[3][4]	10	-	-	uA
		V_{CC}=2.3V; V_I=0.7V	25	-	-	uA
		V_{CC}=3.0V; V_I=0.8V	60	-	-	uA
bus hold HIGH current	I_{BHH}	V_{CC}=1.65V; V_I=1.07V[3][4]	-10	-	-	uA
		V_{CC}=2.3V; V_I=1.7V	-25	-	-	uA
		V_{CC}=3.0V; V_I=2.0V	-60	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	V_{CC}=1.95V[3][5]	200	-	-	uA
		V_{CC}=2.7V	300	-	-	uA
		V_{CC}=3.6V	500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	V_{CC}=1.95V[3][5]	-200	-	-	uA
		V_{CC}=2.7V	-300	-	-	uA
		V_{CC}=3.6V	-500	-	-	uA

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

[2] The bus hold circuit is switched off when V_I>V_{CC} allowing 5.5V on the input pin.

[3] Valid for data inputs (AiP74LVCH16373) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
propagation delay	t_{pd}	Dn to Qn;see Figure 5[2]	V_{CC}=1.2V	-	16.8	-	ns
			V_{CC}=1.65V to 1.95V	1.5	7.6	16.0	ns
			V_{CC}=2.3V to 2.7V	1.0	4.1	8.0	ns
			V_{CC}=2.7V	1.5	4.1	6.9	ns
			V_{CC}=3.0V to 3.6V	1.0	3.4	6.2	ns
		LE to Qn;see Figure 6	V_{CC}=1.2V	-	19.6	-	ns
			V_{CC}=1.65V to 1.95V	2.0	9.0	17.4	ns
			V_{CC}=2.3V to 2.7V	1.5	4.8	8.5	ns
			V_{CC}=2.7V	1.5	4.2	7.4	ns
			V_{CC}=3.0V to 3.6V	1.5	4.1	6.7	ns
enable time	t_{en}	$\overline{OE}$ to Qn;see Figure 7[2]	V_{CC}=1.2V	-	25.2	-	ns
			V_{CC}=1.65V to 1.95V	1.5	7.7	17.4	ns
			V_{CC}=2.3V to 2.7V	1.0	4.3	9.2	ns
			V_{CC}=2.7V	1.5	4.6	8.0	ns
			V_{CC}=3.0V to 3.6V	1.0	3.5	6.9	ns
disable time	t_{dis}	$\overline{OE}$ to Qn;see Figure 7[2]	V_{CC}=1.2V	-	15.4	-	ns
			V_{CC}=1.65V to 1.95V	2.8	6.3	12.7	ns
			V_{CC}=2.3V to 2.7V	1.0	3.5	7.1	ns
			V_{CC}=2.7V	1.5	4.6	8.8	ns
			V_{CC}=3.0V to 3.6V	1.5	4.3	7.6	ns

pulse width	t_W	LE HIGH;see Figure 6	V_{CC}=1.65V to 1.95V	5.0	-	-	ns
			V_{CC}=2.3V to 2.7V	4.0	-	-	ns
			V_{CC}=2.7V	3.0	-	-	ns
			V_{CC}=3.0V to 3.6V	3.0	2.8	-	ns
set-up time	t_{su}	Dn to LE; see Figure 8	V_{CC}=1.65V to 1.95V	3.0	-	-	ns
			V_{CC}=2.3V to 2.7V	2.5	-	-	ns
			V_{CC}=2.7V	2.0	-	-	ns
			V_{CC}=3.0V to 3.6V	2.0	1.4	-	ns
hold time	t_h	Dn to LE; see Figure 8	V_{CC}=1.65V to 1.95V	2.5	-	-	ns
			V_{CC}=2.3V to 2.7V	2.0	-	-	ns
			V_{CC}=2.7V	0.9	-	-	ns
			V_{CC}=3.0V to 3.6V	+0.9	-1.4	-	ns
output skew time	$t_{sk(o)}$	V_{CC}=3.0V to 3.6V[3]		-	-	1.4	ns
power dissipation capacitance	C_{PD}	per input; V_I=GND to V_{CC}[4]	V_{CC}=1.65V to 1.95V	-	15.1	-	pF
			V_{CC}=2.3V to 2.7V	-	18.2	-	pF
			V_{CC}=3.0V to 3.6V	-	21.0	-	pF

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.2V,1.8V,2.5V,2.7V and 3.3V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz; f_o=output frequency in MHz

C_L=output load capacitance in pF

V_{CC}=supply voltage in Volts

N=number of inputs switching

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of the outputs

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
propagation delay	t_{pd}	Dn to Qn;see Figure 5[2]	V_{CC}=1.65V to 1.95V	1.5	-	18.5	ns
			V_{CC}=2.3V to 2.7V	1.0	-	9.2	ns
			V_{CC}=2.7V	1.5	-	9.1	ns
			V_{CC}=3.0V to 3.6V	1.0	-	7.7	ns
		LE to Qn;see Figure 6	V_{CC}=1.65V to 1.95V	2.0	-	20.2	ns
			V_{CC}=2.3V to 2.7V	1.5	-	9.9	ns
			V_{CC}=2.7V	1.5	-	9.8	ns
			V_{CC}=3.0V to 3.6V	1.5	-	8.4	ns
enable time	t_{en}	$\overline{OE}$ to Qn;see Figure 7[2]	V_{CC}=1.65V to 1.95V	1.5	-	20.0	ns
			V_{CC}=2.3V to 2.7V	1.0	-	10.6	ns
			V_{CC}=2.7V	1.5	-	10.5	ns
			V_{CC}=3.0V to 3.6V	1.0	-	9.1	ns
disable time	t_{dis}	$\overline{OE}$ to Qn;see Figure 7[2]	V_{CC}=1.65V to 1.95V	2.8	-	14.7	ns
			V_{CC}=2.3V to 2.7V	1.0	-	8.4	ns
			V_{CC}=2.7V	1.5	-	11.2	ns
			V_{CC}=3.0V to 3.6V	1.5	-	9.8	ns
pulse width	t_W	LE HIGH;see Figure 6	V_{CC}=1.65V to 1.95V	5.0	-	-	ns
			V_{CC}=2.3V to 2.7V	4.0	-	-	ns
			V_{CC}=2.7V	3.0	-	-	ns
			V_{CC}=3.0V to 3.6V	3.0	-	-	ns
set-up time	t_{su}	Dn to LE; see Figure 8	V_{CC}=1.65V to 1.95V	3.0	-	-	ns
			V_{CC}=2.3V to 2.7V	2.5	-	-	ns
			V_{CC}=2.7V	2.0	-	-	ns
			V_{CC}=3.0V to 3.6V	2.0	-	-	ns
hold time	t_h	Dn to LE; see Figure 8	V_{CC}=1.65V to 1.95V	2.5	-	-	ns
			V_{CC}=2.3V to 2.7V	2.0	-	-	ns
			V_{CC}=2.7V	0.9	-	-	ns
			V_{CC}=3.0V to 3.6V	+0.9	-	-	ns
output skew time	$t_{sk(o)}$	V_{CC}=3.0V to 3.6V[3]		-	-	2.1	ns

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.2V,1.8V,2.5V,2.7V and 3.3V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

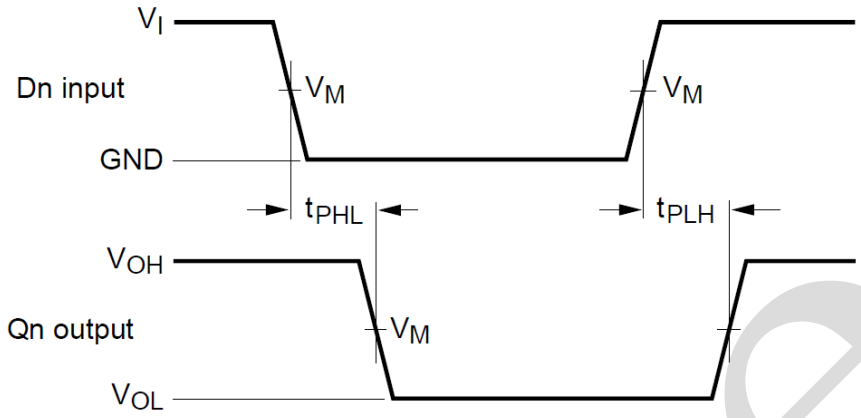
t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

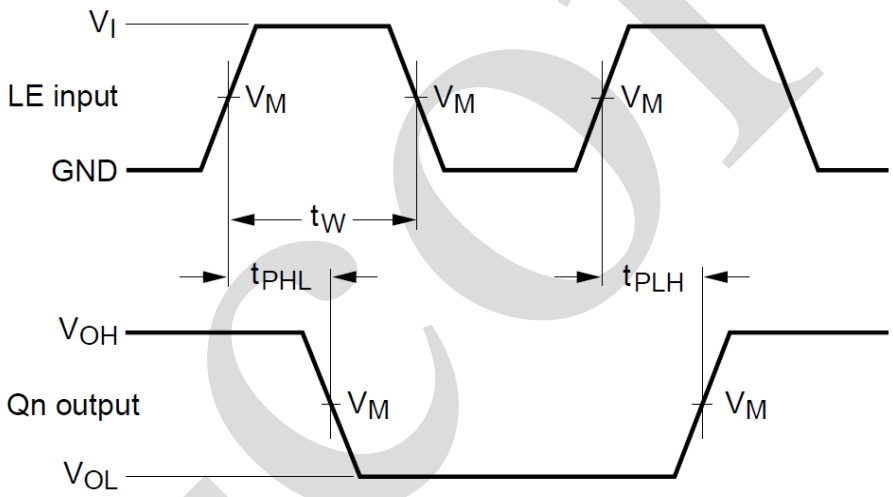
4、Testing Circuit

4.1、AC Testing Waveforms



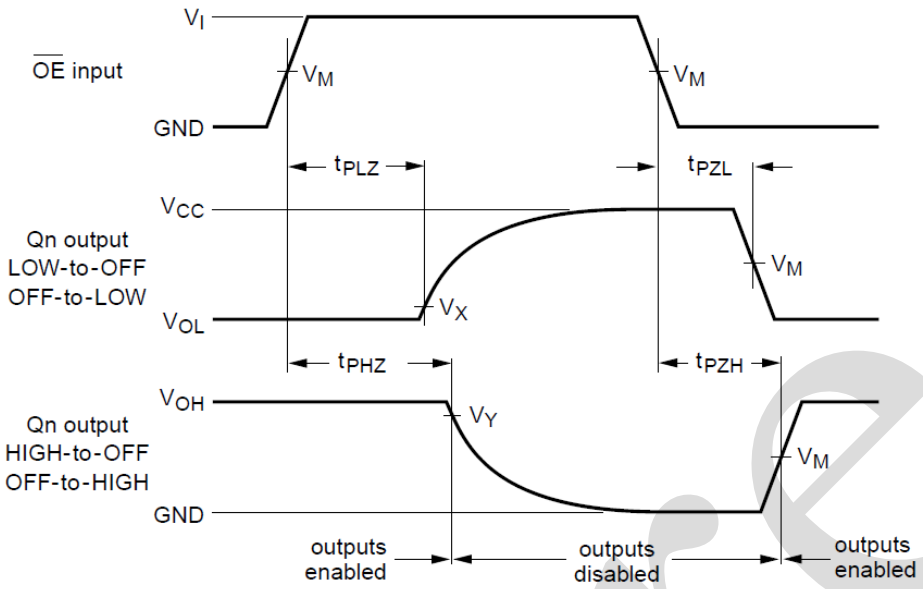
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 5. Input (Dn) to output (Qn) propagation delays



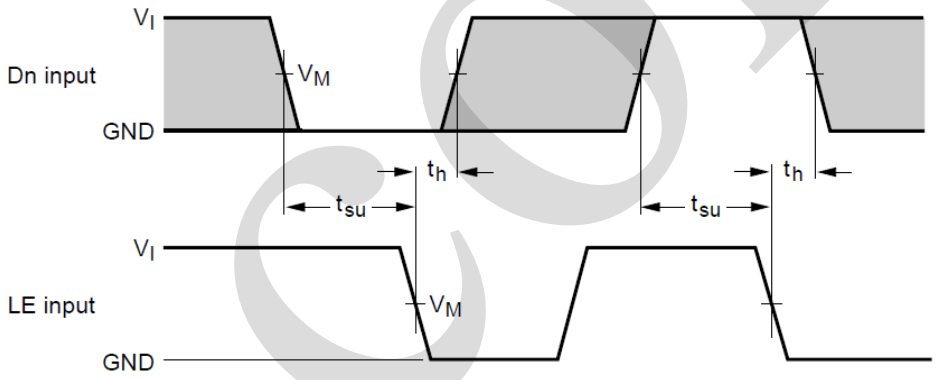
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. Latch enable input (LE) pulse width,
and the latch enable input to output (Qn) propagation delays



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. 3-state enable and disable times



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 8. Data set-up and hold times for the Dn input to the LE input

4.2、Measurement Points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2V	V_{CC}	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
1.65V to 1.95V	V_{CC}	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
2.3V to 2.7V	V_{CC}	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
2.7V	2.7V	1.5V	1.5V	V_{OL}+0.3V	V_{OH}-0.3V
3.0V to 3.6V	2.7V	1.5V	1.5V	V_{OL}+0.3V	V_{OH}-0.3V

4.3、AC Testing Circuit

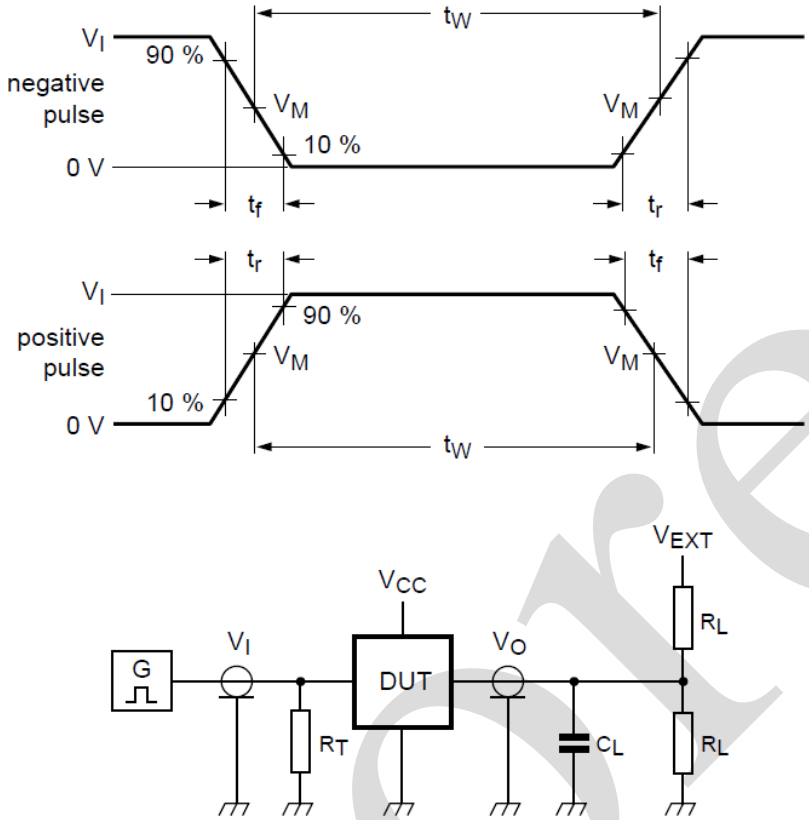


Figure 6. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

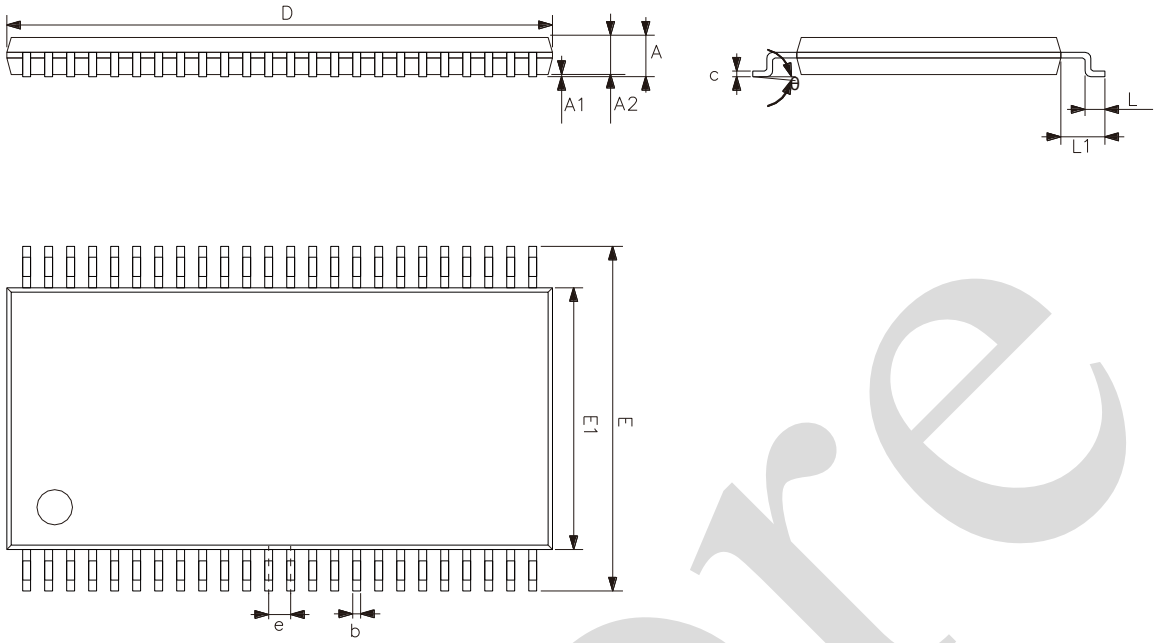
V_{EXT}=External voltage for measuring switching times.

4.4、Test Data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r , t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2V	V_{CC}	≤2ns	30pF	1kΩ	open	2×V_{CC}	GND
1.65V to 1.95V	V_{CC}	≤2ns	30pF	1kΩ	open	2×V_{CC}	GND
2.3V to 2.7V	V_{CC}	≤2ns	30pF	500Ω	open	2×V_{CC}	GND
2.7V	2.7V	≤2.5ns	50pF	500Ω	open	2×V_{CC}	GND
3.0V to 3.6V	2.7V	≤2.5ns	50pF	500Ω	open	2×V_{CC}	GND

5、Package Information

5.1、TSSOP48



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.03	0.15
A2	0.82	1.05
b	0.17	0.27
c	0.12	0.22
D	12.40	12.60
E	7.90	8.30
E1	6.00	6.20
e	0.50	
L	0.35	0.75
L1	1.00	
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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