AiP74LVCH245
Octal Bus Transceiver; 3-State

Product Specification

Specification Revision History：

Version	Date	Description
2025-07-A0	2025-07	New
2026-01-A1	2026-01	Modify the parameters

Contents

1、General Description

The AiP74LVCH245 is an 8-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The AiP74LVCH245 bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

Inputs can be driven from either 3.3V or 5V devices. When disabled, up to 5.5V can be applied to the outputs. This feature allows the use of this device in a mixed 3.3V and 5V environment.

Features:

- 5V tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range from 1.2V to 5.5V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance when V_{CC}=0V
- All data inputs have bus hold
- Specified from -40℃ to +125℃
- Packaging information: SOP20/TSSOP20/DHVQFN20

Ordering Information:

Tube packing specifications:

Type number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVCH245SA20.TB	SOP20	74LVCH245	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVCH245SA20.TR	SOP20	74LVCH245	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74LVCH245TA20.TR	TSSOP20	74LVCH245	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm
AiP74LVCH245QE20.TR	DHVQFN20	74LVCH245	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 4.5mm×2.5mm Pin spacing: 0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

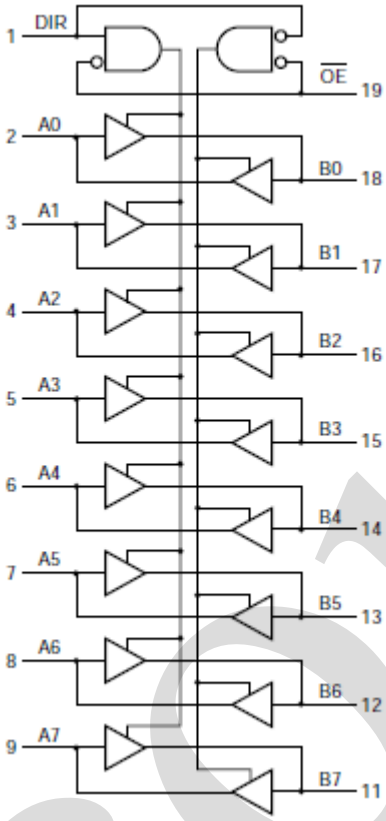


Figure 1. Logic symbol

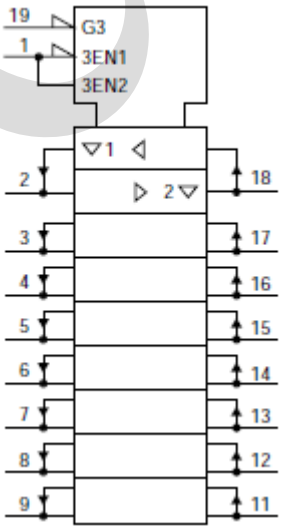


Figure 2. IEC logic symbol

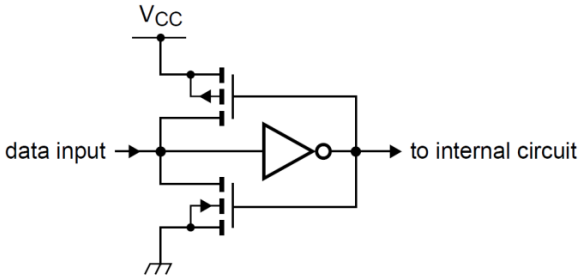
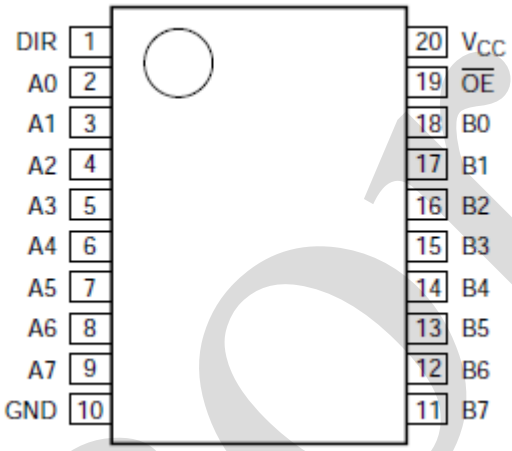


Figure 3. Bus hold circuit

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	DIR	direction control input
2,3,4,5,6,7,8,9	A0 to A7	data input/output
18,17,16,15,14,13,12,11	B0 to B7	data input/output
10	GND	ground (0V)
20	V_{CC}	supply voltage
19	$\overline{OE}$	output enable input (active LOW)

2.4、Function Table

Input		Output	
$\overline{OE}$	DIR	An	Bn
L	L	An = Bn	inputs
L	H	inputs	Bn = An
H	X	Z	Z

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+6.5	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
input voltage	V_I	-[1]	-0.5	+6.5	V
output clamping current	I_{OK}	V_O>V_{CC} or V_O<0V	-	±50	mA
output voltage	V_O	output HIGH or LOW state[2]	-0.5	V_{CC}+0.5	V
		output 3-state[2]	-0.5	+6.5	V
output current	I_O	V_O=0V to V_{CC}	-	±50	mA
supply current	I_{CC}	-	-	100	mA
ground current	I_{GND}	-	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total power dissipation	P_{tot}	-	-	500	mW
soldering temperature	T_L	10s	260		℃
electrostatic discharge	ESD	HBM	2000		V
		CDM	1000		V

Note:

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	1.65	-	5.5	V
		functional	1.2	-	5.5	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃
input transition rise and fall rate	Δt/ΔV	V_{CC}=1.2V to 2.7V	0	-	20	ns/V
		V_{CC}=2.7V to 3.6V	0	-	10	ns/V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65×V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7×V_{CC}	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3×V_{CC}	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 3.6V	V_{CC}-0.2	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.2	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.8	-	-	V
			I_O=-12mA; V_{CC}=2.7V	2.2	-	-	V
			I_O=-18mA; V_{CC}=3.0V	2.4	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.2	-	-	V
			I_O=-32mA; V_{CC}=4.5V	3.8	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 3.6V	-	-	0.2	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.45	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.6	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.4	V
			I_O=24mA; V_{CC}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CC}=4.5V	-	-	0.55	V
input leakage current[2]	I_I	V_I=5.5V or GND; V_{CC}=3.6V		-	-	±5	uA
OFF-state output current[2][3]	I_{OZ}	V_I=V_{IH} or V_{IL}; V_O=5.5V or GND; V_{CC}=3.6V		-	-	±5	uA
power-off leakage current	I_{OFF}	V_I or V_O=5.5V; V_{CC}=0V		-	-	±10	uA
supply current	I_{CC}	V_I=V_{CC} or GND;I_O=0A; V_{CC}=3.6V		-	-	20	uA
additional supply current	ΔI_{CC}	per input pin;V_I=V_{CC}-0.6V; I_O=0A;V_{CC}=2.7V to 3.6V;		-	-	500	uA
input capacitance	C_I	V_{CC}=0V to 3.6V; V_I=GND to V_{CC}		-	5	-	pF
input/output capacitance	$C_{I/O}$	V_{CC}=0V to 3.6V; V_I=GND to V_{CC}		-	10	-	pF
bus hold LOW	I_{BHL}	V_{CC}=1.65V; V_I=0.58V		10	-	-	uA
		V_{CC}=2.3V; V_I=0.7V		30	-	-	uA

current[4][5]		V_{CC}=3.0V; V_I=0.8V	75	-	-	uA
bus hold HIGH current[4][5]	I_{BHH}	V_{CC}=1.65V; V_I=1.07V	-10	-	-	uA
		V_{CC}=2.3V; V_I=1.7V	-30	-	-	uA
		V_{CC}=3.0V; V_I=2.0V	-75	-	-	uA
bus hold LOW overdrive current[4][6]	I_{BHLO}	V_{CC}=1.95V	200	-	-	uA
		V_{CC}=2.7V	300	-	-	uA
		V_{CC}=3.6V	500	-	-	uA
bus hold HIGH overdrive current[4][6]	I_{BHHO}	V_{CC}=1.95V	-200	-	-	uA
		V_{CC}=2.7V	-300	-	-	uA
		V_{CC}=3.6V	-500	-	-	uA

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

[2] The bus hold circuit is switched off when V_I>V_{CC} allowing 5.5V on the input terminal.

[3] For I/O ports the parameter I_{OZ} includes the input leakage current.

[4] Valid for data inputs. Note that control inputs do not have a bus hold circuit.

[5] The specified sustaining current at the data input holds the input below the specified V_I level.

[6] The specified overdrive current at the data input forces the data input to the opposite logic input state.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65×V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
		V_{CC}=4.5V to 5.5V		0.7×V_{CC}	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
		V_{CC}=4.5V to 5.5V		-	-	0.3×V_{CC}	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 3.6V	V_{CC}-0.3	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.05	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.65	-	-	V
			I_O=-12mA; V_{CC}=2.7V	2.05	-	-	
			I_O=-18mA; V_{CC}=3.0V	2.25	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.0	-	-	V
			I_O=-32mA; V_{CC}=4.5V	3.4	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 3.6V	-	-	0.3	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.65	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.8	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.6	V
			I_O=24mA; V_{CC}=3.0V	-	-	0.8	V

		I_O=32mA; V_{CC}=4.5V	-	-	0.8	V
input leakage current[2]	I_I	V_I=5.5V or GND; V_{CC}=3.6V	-	-	±20	uA
OFF-state output current[2][3]	I_{OZ}	V_I=V_{IH} or V_{IL}; V_O=5.5V or GND; V_{CC}=3.6V	-	-	±20	uA
power-off leakage current	I_{OFF}	V_I or V_O=5.5V; V_{CC}=0V	-	-	±20	uA
supply current	I_{CC}	V_I=V_{CC} or GND;I_O=0A; V_{CC}=3.6V	-	-	80	uA
additional supply current	ΔI_{CC}	per input pin;V_I=V_{CC}-0.6V; I_O=0A;V_{CC}=2.7V to 3.6V;	-	5	5000	uA
bus hold LOW current[4][5]	I_{BHL}	V_{CC}=1.65V; V_I=0.58V	10	-	-	uA
		V_{CC}=2.3V; V_I=0.7V	25	-	-	uA
		V_{CC}=3.0V; V_I=0.8V	60	-	-	uA
bus hold HIGH current[4][5]	I_{BHH}	V_{CC}=1.65V; V_I=1.07V	-10	-	-	uA
		V_{CC}=2.3V; V_I=1.7V	-25	-	-	uA
		V_{CC}=3.0V; V_I=2.0V	-60	-	-	uA
bus hold LOW overdrive current[4][6]	I_{BHLO}	V_{CC}=1.95V	200	-	-	uA
		V_{CC}=2.7V	300	-	-	uA
		V_{CC}=3.6V	500	-	-	uA
bus hold HIGH overdrive current[4][6]	I_{BHHO}	V_{CC}=1.95V	-200	-	-	uA
		V_{CC}=2.7V	-300	-	-	uA
		V_{CC}=3.6V	-500	-	-	uA

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

[2] The bus hold circuit is switched off when V_I>V_{CC} allowing 5.5V on the input terminal.

[3] For I/O ports the parameter I_{OZ} includes the input leakage current.

[4] Valid for data inputs. Note that control inputs do not have a bus hold circuit.

[5] The specified sustaining current at the data input holds the input below the specified V_I level.

[6] The specified overdrive current at the data input forces the data input to the opposite logic input state.

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[2]	Max.	Unit
propagation delay	t_{pd}	An to Bn; Bn to An; see Figure 4[1]	V_{CC}=1.2V	-	17.0	-	ns
			V_{CC}=1.65V to 1.95V	1.5	6.5	14.6	ns
			V_{CC}=2.3V to 2.7V	1.0	3.4	7.6	ns
			V_{CC}=2.7V	1.5	3.4	7.3	ns
			V_{CC}=3.0V to 3.6V	1.5	2.9	6.3	ns
			V_{CC}=4.5V to 5.5V	1.5	2.5	5.5	ns
enable time	t_{en}	$\overline{OE}$ to An,Bn; see Figure 5[1]	V_{CC}=1.2V	-	22.0	-	ns
			V_{CC}=1.65V to 1.95V	1.9	8.3	19.5	ns
			V_{CC}=2.3V to 2.7V	1.5	4.6	10.7	ns
			V_{CC}=2.7V	1.5	4.8	9.5	ns
			V_{CC}=3.0V to 3.6V	1.5	3.7	8.5	ns
			V_{CC}=4.5V to 5.5V	1.5	3.2	7.4	ns
disable time	t_{dis}	$\overline{OE}$ to An,Bn; see Figure 5[1]	V_{CC}=1.2V	-	12.0	-	ns
			V_{CC}=1.65V to 1.95V	2.9	5.5	12.3	ns
			V_{CC}=2.3V to 2.7V	1.0	3.1	7.1	ns
			V_{CC}=2.7V	1.5	3.9	8.0	ns
			V_{CC}=3.0V to 3.6V	1.7	3.6	7.0	ns
			V_{CC}=4.5V to 5.5V	1.7	3.1	6.1	ns
power dissipation capacitance	C_{PD}	per input; V_I=GND to V_{CC}[3]	V_{CC}=1.65V to 1.95V	-	7.7	-	pF
			V_{CC}=2.3V to 2.7V	-	11.3	-	pF
			V_{CC}=3.0V to 3.6V	-	14.4	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.2V, 1.8V, 2.5V, 2.7V, 3.3V and 5V respectively.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz; f_o=output frequency in MHz

C_L=output load capacitance in pF

V_{CC}=supply voltage in Volts

N=number of inputs switching

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of the outputs

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[2]	Max.	Unit
propagation delay	t_{pd}	An to Bn; Bn to An; see Figure 4[1]	V_{CC}=1.65V to 1.95V	1.5	-	16.9	ns
			V_{CC}=2.3V to 2.7V	1.0	-	8.7	ns
			V_{CC}=2.7V	1.5	-	9.5	ns
			V_{CC}=3.0V to 3.6V	1.5	-	8.0	ns
			V_{CC}=4.5V to 5.5V	1.5	-	7.0	ns
enable time	t_{en}	$\overline{OE}$ to An,Bn; see Figure 5[1]	V_{CC}=1.65V to 1.95V	1.9	-	22.5	ns
			V_{CC}=2.3V to 2.7V	1.5	-	12.4	ns
			V_{CC}=2.7V	1.5	-	12.0	ns
			V_{CC}=3.0V to 3.6V	1.5	-	11.0	ns
			V_{CC}=4.5V to 5.5V	1.5	-	9.6	ns
disable time	t_{dis}	$\overline{OE}$ to An,Bn; see Figure 5[1]	V_{CC}=1.65V to 1.95V	2.9	-	14.2	ns
			V_{CC}=2.3V to 2.7V	1.0	-	8.2	ns
			V_{CC}=2.7V	1.5	-	10.0	ns
			V_{CC}=3.0V to 3.6V	1.7	-	9.0	ns
			V_{CC}=4.5V to 5.5V	1.7	-	7.8	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

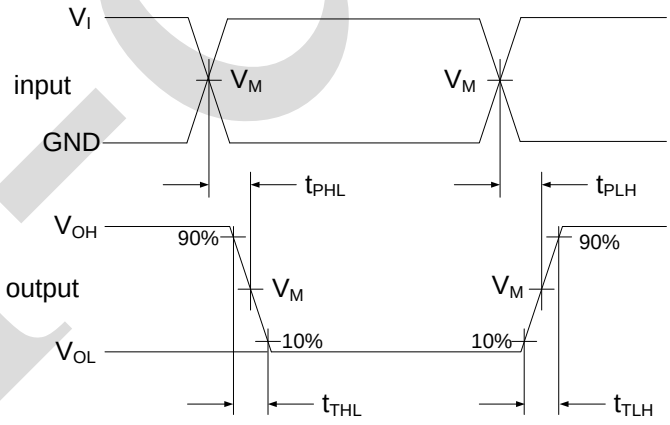
t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.2V, 1.8V, 2.5V, 3.3V and 5V respectively.

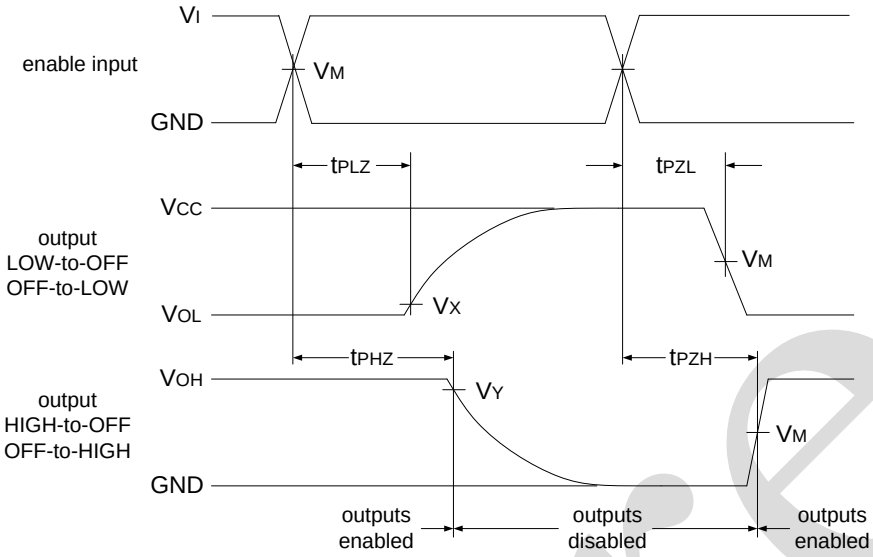
4、Testing Circuit

4.1、AC Testing Waveforms



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. The input (An, Bn) to output (Bn, An) propagation delays



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 5. 3-state enable and disable times

4.2、Measurement Points

Supply voltage	**V_M**	**Input**			
V_{CC}		**V_I**	**t_r=t_f**	**V_X**	**V_Y**
1.2V	0.5×V_{CC}	V_{CC}	≤2.5ns	V_{OL}+0.15V	V_{OH}-0.15V
1.65V to 1.95V	0.5×V_{CC}	V_{CC}	≤2.5ns	V_{OL}+0.15V	V_{OH}-0.15V
2.3V to 2.7V	0.5×V_{CC}	V_{CC}	≤2.5ns	V_{OL}+0.15V	V_{OH}-0.15V
2.7V	1.5V	2.7V	≤2.5ns	V_{OL}+0.3V	V_{OH}-0.3V
3.0V to 3.6V	1.5V	2.7V	≤2.5ns	V_{OL}+0.3V	V_{OH}-0.3V

4.3、AC Testing Circuit

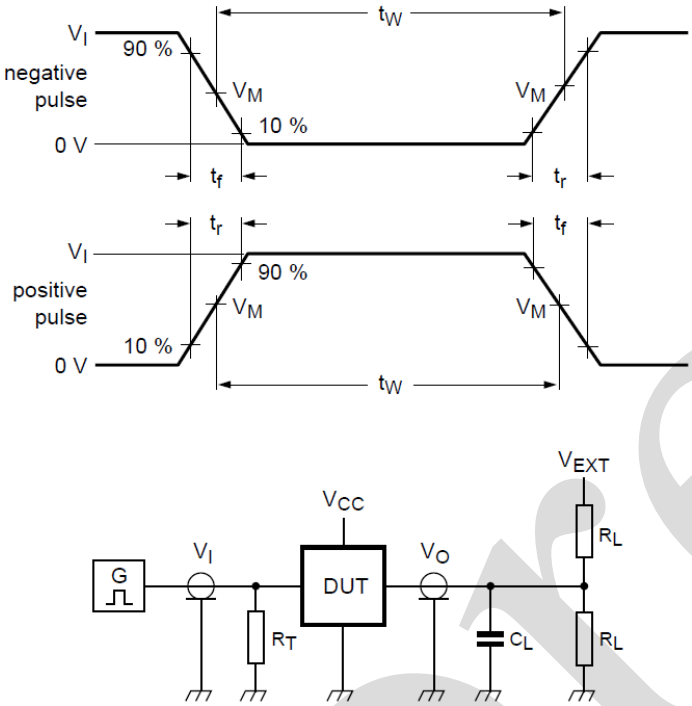


Figure 6. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

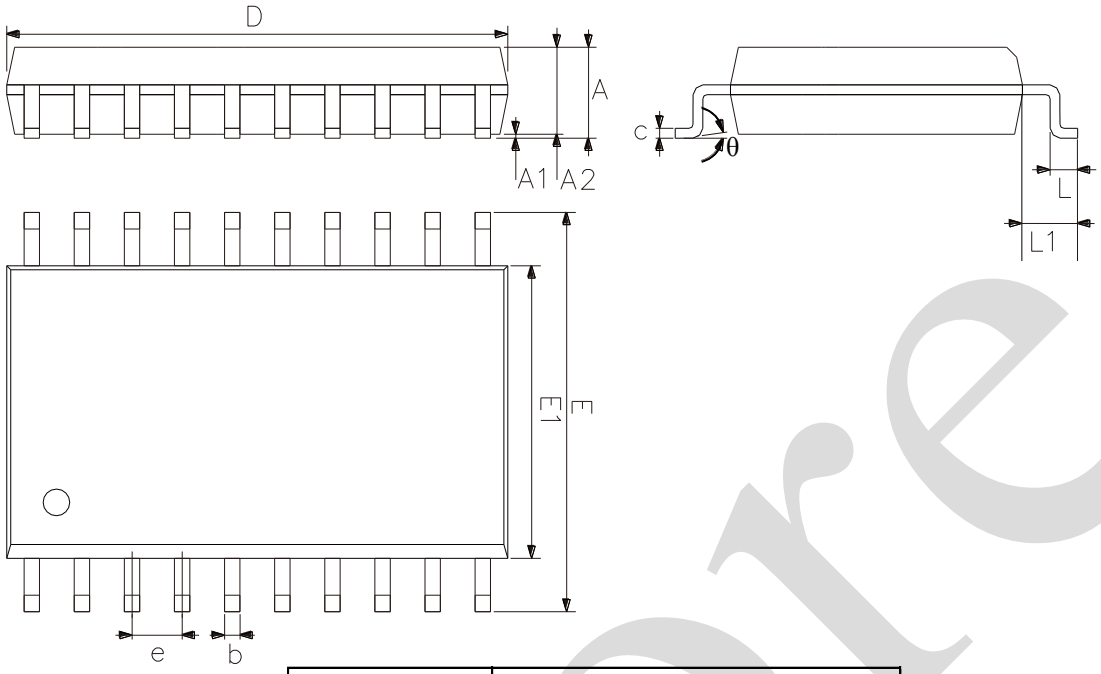
V_{EXT}=External voltage for measuring switching times.

4.4、Test Data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r , t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2V	V_{CC}	≤2ns	30pF	1kΩ	open	2×V_{CC}	GND
1.65V to 1.95V	V_{CC}	≤2ns	30pF	1kΩ	open	2×V_{CC}	GND
2.3V to 2.7V	V_{CC}	≤2ns	30pF	500Ω	open	2×V_{CC}	GND
2.7V	2.7V	≤2.5ns	50pF	500Ω	open	2×V_{CC}	GND
3.0V to 3.6V	2.7V	≤2.5ns	50pF	500Ω	open	2×V_{CC}	GND

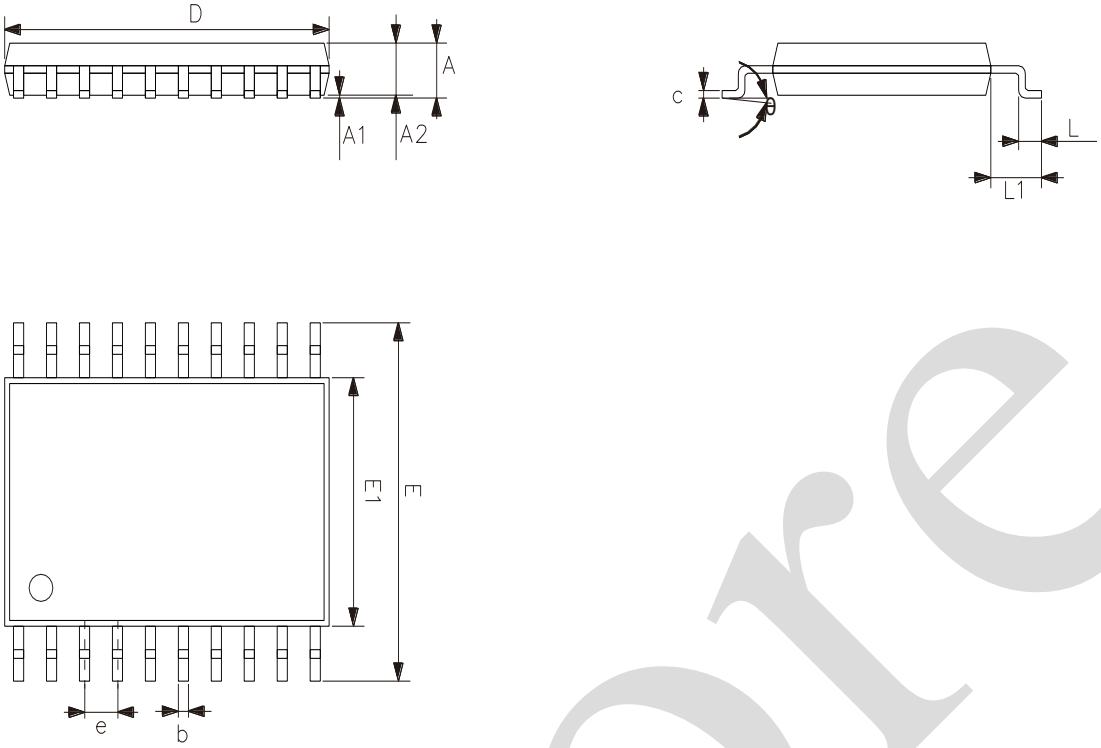
5、Package Information

5.1、SOP20



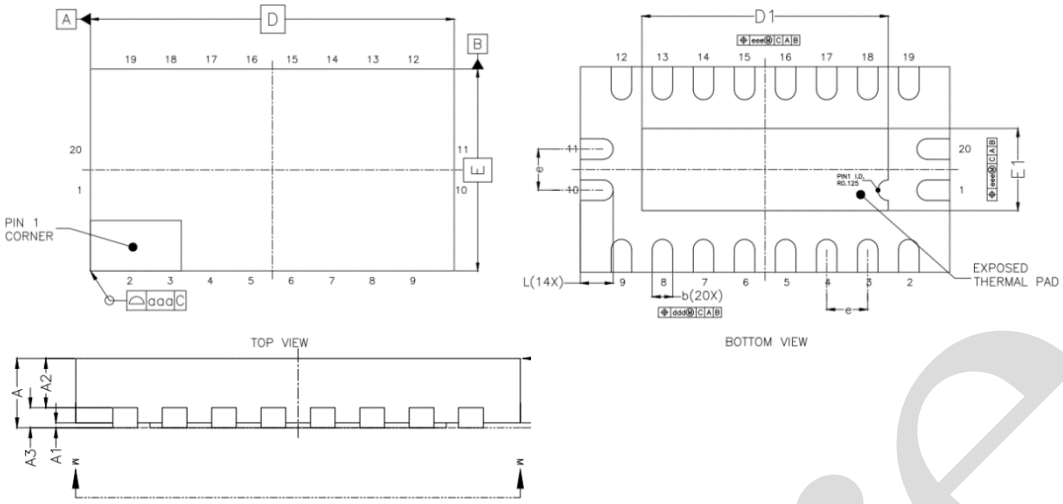
2023/12/A	Dimensions In Millimeters	
Symbol	**Min.**	**Max.**
A	2.47	2.65
A1	0.05	0.30
A2	2.20	2.44
b	0.35	0.50
c	0.15	0.30
D	12.54	12.94
E	10.00	10.60
E1	7.30	7.70
e	1.27	
L	0.40	1.05
L1	1.30	1.50
θ	0°	8°

5.2、TSSOP20



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

5.3、DHVQFN20



2023/12/A	Dimensions In Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.70
A3	0.20	
D	4.40	4.60
E	2.40	2.60
e	0.50	
b	0.18	0.30
L	0.30	0.50
D1	2.70	3.15
E1	0.70	1.15

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We recommend you to read this chapter carefully before using this product.

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