AiP74LVC573
Octal D-type transparent latch with 5V tolerant inputs/outputs; 3-state

Product Specification

Specification Revision History：

Version	Date	Description
2017-04-A1	2017-04	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description 3
2、Block Diagram And Pin Description 5
2.1、Block Diagram 5
2.2、Pin Configurations 6
2.3、Pin Description 6
2.4、Function Table 7
3、Electrical Parameter 7
3.1、Absolute Maximum Ratings 7
3.2、Recommended Operating Conditions 8
3.3、Electrical Characteristics 8
3.3.1、DC Characteristics 1 8
3.3.2、DC Characteristics 2 9
3.3.3、AC Characteristics 1 10
3.3.4、AC Characteristics 2 12
4、Testing Circuit 13
4.1、AC Testing Circuit 13
4.2、Test Data 13
4.3、AC Testing Waveforms 14
4.4、Measurement Points 15
5、Package Information 16
5.1、SOP20 16
5.2、TSSOP20 17
5.3、DHVQFN20 18
6、Statements And Notes 19
6.1、The name and content of Hazardous substances or Elements in the product 19
6.2、Notes 19

1、General Description

The AiP74LVC573 consists of eight D-type transparent latches, featuring separate D-type inputs for each latch and 3-state true outputs for bus-oriented applications. A Latch Enable (LE) input and an Output Enable ($\overline{OE}$) input are common to all internal latches.

When LE is HIGH, data at the Dn inputs enters the latches. In this condition, the latches are transparent, that is, a latch output changes each time its corresponding D-input changes. When LE is LOW, the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of LE.

When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

Inputs can be driven from either 3.3V or 5V devices. When disabled, up to 5.5V can be applied to the outputs. These features allow the use of these devices as translators in mixed 3.3V or 5V applications.

The AiP74LVC573 is functionally identical to the AiP74LVC373, but has a different pin arrangement.

Features:

- 5V tolerant inputs/outputs, for interfacing with 5V logic
- Supply voltage range from 1.2V to 3.6V
- CMOS low power consumption
- Direct interface with TTL levels
- High-impedance when V_{CC}=0V
- Flow-through pinout architecture
- Specified from -40℃ to +125℃
- Packaging information:SOP20/TSSOP20/DHVQFN20

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVC573SA20.TB	SOP20	74LVC573	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74LVC573TA20.TB	TSSOP20	74LVC573	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVC573SA20.TR	SOP20	74LVC573	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
AiP74LVC573TA20.TR	TSSOP20	74LVC573	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm
AiP74LVC573QE20.TR	DHVQFN20	74LVC573	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 4.5mm×2.5mm Pin spacing:0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

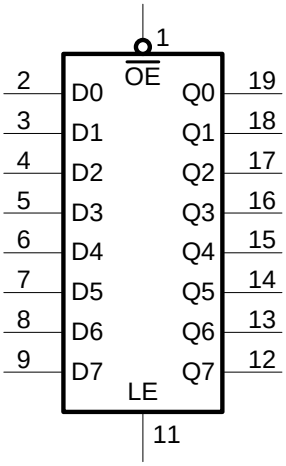


Figure 1. Logic symbol

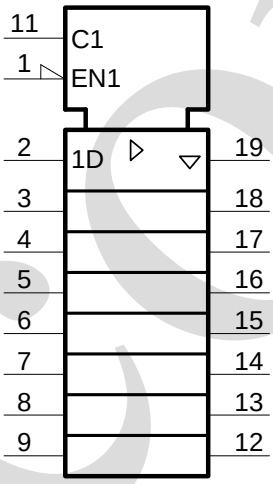


Figure 2. IEC logic symbol

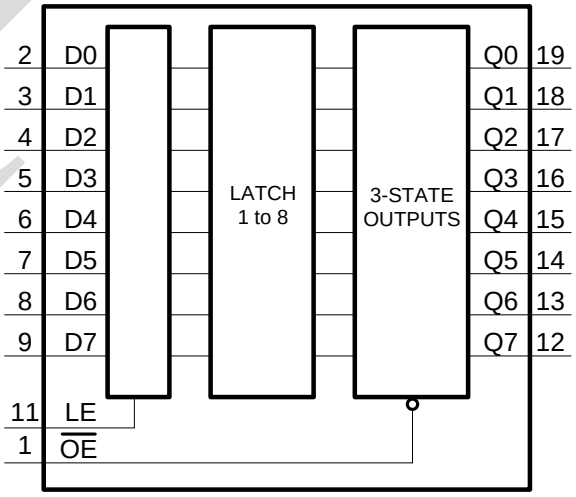


Figure 3. Functional diagram

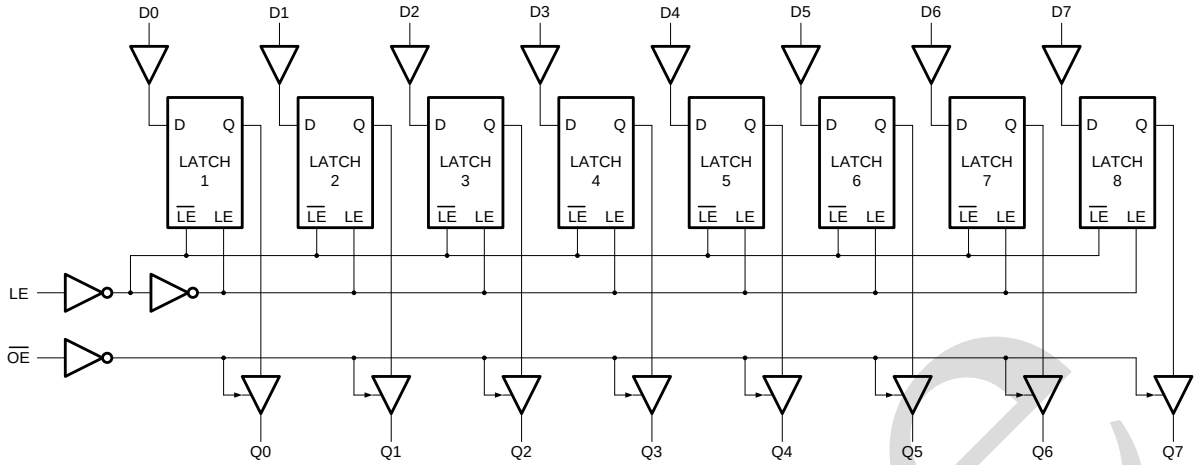
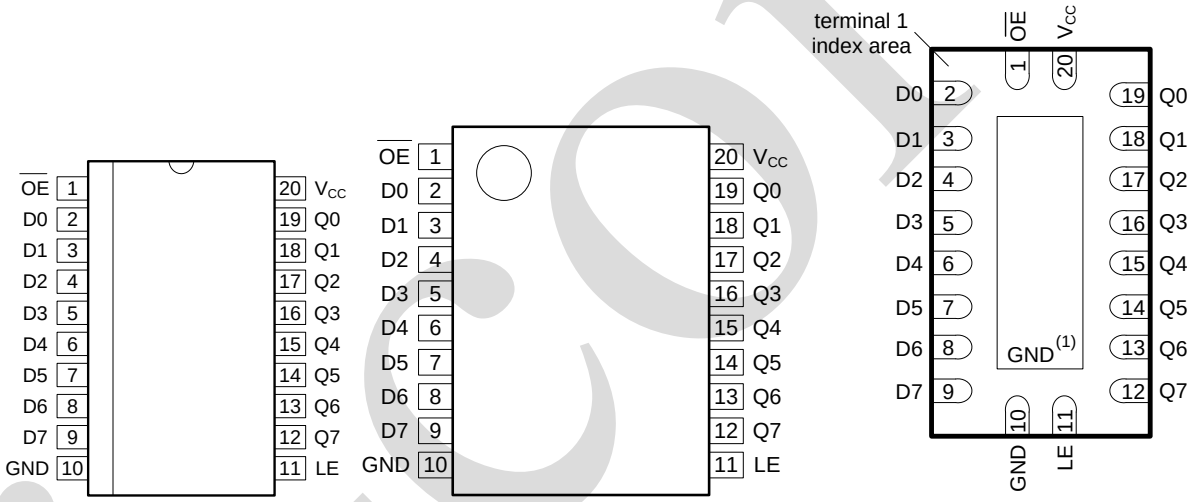


Figure 4. Logic diagram

2.2、Pin Configurations



SOP20 **TSSOP20** **DHVQFN20**

Note: (1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

2.3、Pin Description

Pin No.	Pin Name	Description
1	$\overline{OE}$	output enable input (active LOW)
2	D0	data input
3	D1	data input
4	D2	data input
5	D3	data input
6	D4	data input
7	D5	data input
8	D6	data input

9	D7	data input
10	GND	ground (0V)
11	LE	latch enable input (active HIGH)
12	Q7	data output
13	Q6	data output
14	Q5	data output
15	Q4	data output
16	Q3	data output
17	Q2	data output
18	Q1	data output
19	Q0	data output
20	V_{CC}	supply voltage

2.4、Function Table

Operating modes	Input			Internal latch	Output
	$\overline{OE}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Note:
H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high-impedance OFF-state

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified)

Characteristic	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+6.5	V
input clamping current	I_{IK}	$V_I < 0V$	-50	-	mA
input voltage	V_I	-[1]	-0.5	+6.5	V
output clamping current	I_{OK}	$V_O>V_{CC}$ or $V_O<0V$	-	±50	mA
output voltage	V_O	-[2]	-0.5	V_{CC}+0.5	V
output current	I_O	V_O=0V to V_{CC}	-	±50	mA
supply current	I_{CC}	-	-	100	mA
ground current	I_{GND}	-	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
total power dissipation	P_{tot}	-	-	500	mW
Soldering Temperature	T_L	10s	260		℃

Note:

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	1.65	-	3.6	V
		functional	1.2	-	-	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃
input transition rise and fall rate	$\Delta t/\Delta V$	V_{CC}= 1.65V to 2.7V	0	-	20	ns/V
		V_{CC}= 2.7V to 3.6V	0	-	10	ns/V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65×V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 3.6V	V_{CC}-0.2	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.2	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.8	-	-	V
			I_O=-12mA; V_{CC}=2.7V	2.2	-	-	V
			I_O=-18mA; V_{CC}=3.0V	2.4	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.2	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 3.6V	-	-	0.2	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.45	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.6	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.4	V

			I_O=24mA; V_{CC}=3.0V	-	-	0.55	V
input leakage current	I_I	V_{CC}=3.6V; V_I=5.5V or GND		-	-	±5	uA
OFF-state output current	I_{OZ}	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}; V_O=5.5V or GND		-	-	±5	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=5.5V		-	-	±10	uA
supply current	I_{CC}	V_{CC}=3.6V; V_I=V_{CC} or GND; I_O=0A		-	-	10	uA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=2.7V to 3.6V; V_I= V_{CC}-0.6V; I_O=0A		-	-	500	uA
input capacitance	C_I	V_{CC}=0V to 3.6V;V_I=GND to V_{CC}		-	5	-	pF

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65×V_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 3.6V	V_{CC}-0.3	-	-	V
			I_O=-4mA; V_{CC}=1.65V	1.05	-	-	V
			I_O=-8mA; V_{CC}=2.3V	1.65	-	-	V
			I_O=-12mA; V_{CC}=2.7V	2.05	-	-	V
			I_O=-18mA; V_{CC}=3.0V	2.25	-	-	V
			I_O=-24mA; V_{CC}=3.0V	2.0	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 3.6V	-	-	0.3	V
			I_O=4mA; V_{CC}=1.65V	-	-	0.65	V
			I_O=8mA; V_{CC}=2.3V	-	-	0.8	V
			I_O=12mA; V_{CC}=2.7V	-	-	0.6	V

			I_O=24mA; V_{CC}=3.0V	-	-	0.8	V
input leakage current	I_I	V_{CC}=3.6V; V_I=5.5V or GND		-	-	±20	uA
OFF-state output current	I_{OZ}	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}; V_O=5.5V or GND		-	-	±20	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=5.5V		-	-	±20	uA
supply current	I_{CC}	V_{CC}=3.6V; V_I=V_{CC} or GND; I_O=0A		-	-	40	uA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=2.7V to 3.6V; V_I= V_{CC}-0.6V; I_O=0A		-	-	5000	uA

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25℃.

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
propagation delay	t_{pd}	Dn to Qn; see Figure 6[2]	V_{CC}=1.2V	-	16.0	-	ns
			V_{CC}=1.65V to 1.95V	2.1	7.8	16.3	ns
			V_{CC}=2.3V to 2.7V	1.5	4.1	8.0	ns
			V_{CC}=2.7V	1.5	4.1	7.2	ns
			V_{CC}=3.0V to 3.6V	1.5	3.4	6.2	ns
		LE to Qn; see Figure 7[2]	V_{CC}=1.2V	-	16.0	-	ns
			V_{CC}=1.65V to 1.95V	2.0	7.7	16.0	ns
			V_{CC}=2.3V to 2.7V	1.5	4.1	7.8	ns
			V_{CC}=2.7V	1.5	3.7	7.5	ns
			V_{CC}=3.0V to 3.6V	1.5	3.4	6.5	ns
enable time	t_{en}	$\overline{OE}$ to Qn; see Figure 8[2]	V_{CC}=1.2V	-	18.0	-	ns
			V_{CC}=1.65V to 1.95V	1.7	7.5	17.5	ns
			V_{CC}=2.3V to 2.7V	1.5	4.2	9.2	ns
			V_{CC}=2.7V	1.5	4.2	8.5	ns
			V_{CC}=3.0V to 3.6V	1.5	3.4	7.5	ns
disable time	t_{dis}	$\overline{OE}$ to Qn; see Figure 8[2]	V_{CC}=1.2V	-	8.0	-	ns
			V_{CC}=1.65V to 1.95V	1.0	3.3	10.1	ns
			V_{CC}=2.3V to 2.7V	0.3	1.8	5.7	ns
			V_{CC}=2.7V	1.5	3.0	6.5	ns
			V_{CC}=3.0V to 3.6V	1.5	2.5	6.0	ns
pulse width	t_W	LE HIGH; see Figure 7	V_{CC}=1.65V to 1.95V	5.0	-	-	ns
			V_{CC}=2.3V to 2.7V	4.0	-	-	ns
			V_{CC}=2.7V	3.2	-	-	ns
			V_{CC}=3.0V to 3.6V	3.2	1.6	-	ns
set-up time	t_{su}	Dn to LE; see Figure 9	V_{CC}=1.65V to 1.95V	4.0	-	-	ns
			V_{CC}=2.3V to 2.7V	2.5	-	-	ns
			V_{CC}=2.7V	1.7	-	-	ns
			V_{CC}=3.0V to 3.6V	1.7	-	-	ns

hold time	t_h	Dn to LE; see Figure 9	V_{CC}=1.65V to 1.95V	3.0	-	-	ns
			V_{CC}=2.3V to 2.7V	1.9	-	-	ns
			V_{CC}=2.7V	1.5	-	-	ns
			V_{CC}=3.0V to 3.6V	1.4	-	-	ns
output skew time	$t_{sk(o)}$	V_{CC}=3.0V to 3.6V[3]		-	-	1.0	ns
power dissipation capacitance	C_{PD}	per latch; V_I= GND to V_{CC}[4]	V_{CC}= 1.65V to 1.95V	-	7.1	-	pF
			V_{CC}= 2.3V to 2.7V	-	10.3	-	
			V_{CC}=3.0V to 3.6V	-	13.2	-	

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.2V, 1.8V, 2.5V, 2.7V, and 3.3V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZH} and t_{PZL}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:
f_i=input frequency in MHz; f_o=output frequency in MHz
C_L=output load capacitance in pF
V_{CC}=supply voltage in Volts
N=number of inputs switching
$\sum(C_L\times V_{CC}^2\times f_o)$=sum of the outputs

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
propagation delay	t_{pd}	Dn to Qn; see Figure 6[2]	V_{CC}=1.65V to 1.95V	2.1	-	18.8	ns
			V_{CC}=2.3V to 2.7V	1.5	-	9.2	ns
			V_{CC}=2.7V	1.5	-	9.0	ns
			V_{CC}=3.0V to 3.6V	1.5	-	8.0	ns
		LE to Qn; see Figure 7[2]	V_{CC}=1.65V to 1.95V	2.0	-	18.4	ns
			V_{CC}=2.3V to 2.7V	1.5	-	9.1	ns
			V_{CC}=2.7V	1.5	-	9.5	ns
			V_{CC}=3.0V to 3.6V	1.5	-	8.5	ns
enable time	t_{en}	$\overline{OE}$ to Qn; see Figure 8[2]	V_{CC}=1.65V to 1.95V	1.7	-	20.2	ns
			V_{CC}=2.3V to 2.7V	1.5	-	10.6	ns
			V_{CC}=2.7V	1.5	-	11.0	ns
			V_{CC}=3.0V to 3.6V	1.5	-	9.5	ns
disable time	t_{dis}	$\overline{OE}$ to Qn; see Figure 8[2]	V_{CC}=1.65V to 1.95V	1.0	-	11.6	ns
			V_{CC}=2.3V to 2.7V	0.3	-	6.6	ns
			V_{CC}=2.7V	1.5	-	8.5	ns
			V_{CC}=3.0V to 3.6V	1.5	-	7.5	ns
pulse width	t_W	LE HIGH; see Figure 7	V_{CC}=1.65V to 1.95V	5.0	-	-	ns
			V_{CC}=2.3V to 2.7V	4.0	-	-	ns
			V_{CC}=2.7V	3.2	-	-	ns
			V_{CC}=3.0V to 3.6V	3.2	-	-	ns
set-up time	t_{su}	Dn to LE; see Figure 9	V_{CC}=1.65V to 1.95V	4.0	-	-	ns
			V_{CC}=2.3V to 2.7V	2.5	-	-	ns
			V_{CC}=2.7V	1.7	-	-	ns
			V_{CC}=3.0V to 3.6V	1.7	-	-	ns
hold time	t_h	Dn to LE; see Figure 9	V_{CC}=1.65V to 1.95V	3.0	-	-	ns
			V_{CC}=2.3V to 2.7V	1.9	-	-	ns
			V_{CC}=2.7V	1.5	-	-	ns
			V_{CC}=3.0V to 3.6V	1.4	-	-	ns
output skew time	$t_{sk(o)}$	V_{CC}=3.0V to 3.6V[3]		-	-	1.5	ns

Note:

[1] Typical values are measured at T_{amb}=25℃ and V_{CC}=1.2V, 1.8V, 2.5V, 2.7V, and 3.3V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZH} and t_{PZL}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

4、Testing Circuit

4.1、AC Testing Circuit

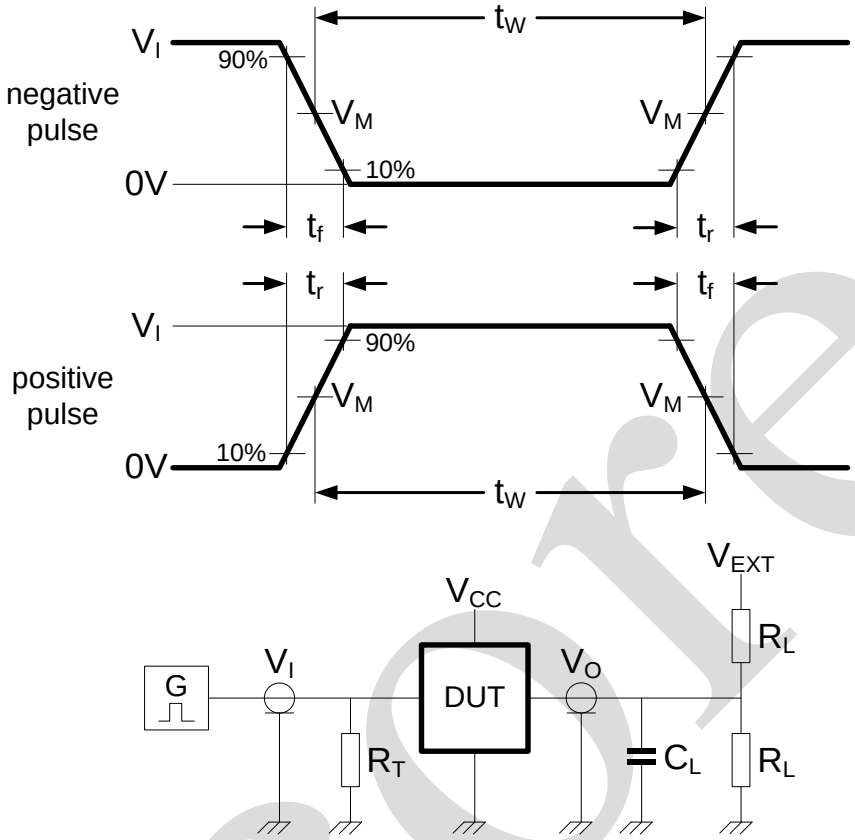


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

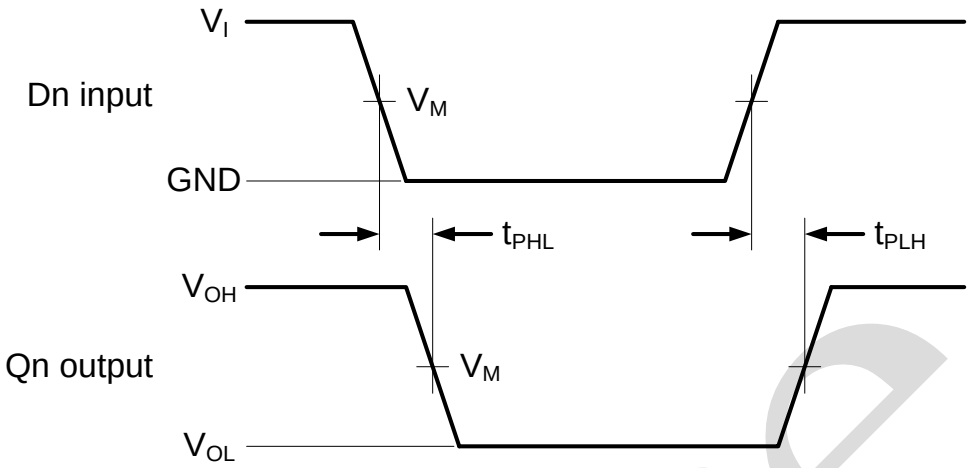
R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT}=External voltage for measuring switching times.

4.2、Test Data

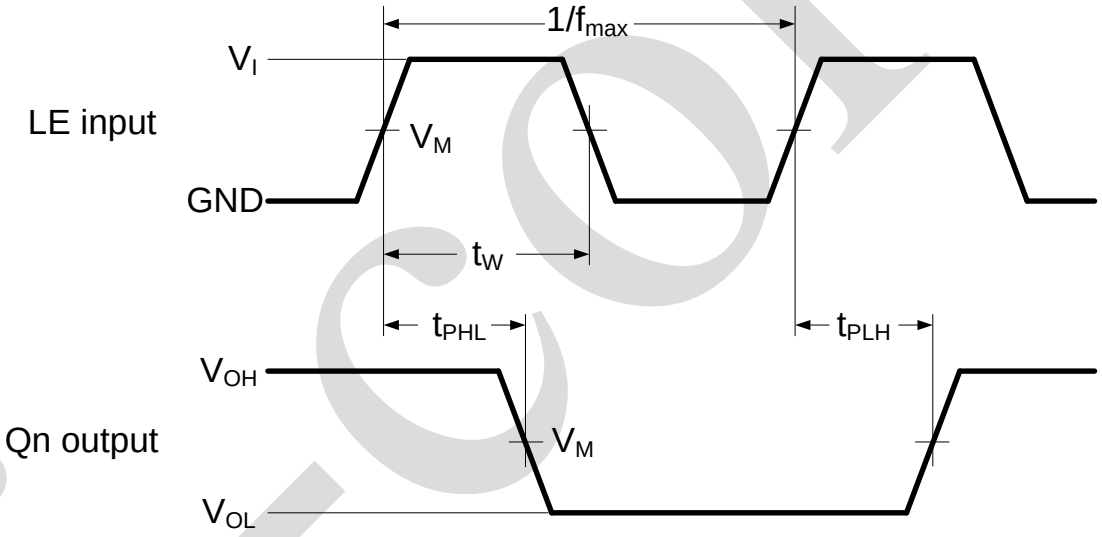
Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2V	V_{CC}	≤2.0ns	30pF	1kΩ	open	2×V_{CC}	GND
1.65V to 1.95V	V_{CC}	≤2.0ns	30pF	1kΩ	open	2×V_{CC}	GND
2.3V to 2.7V	V_{CC}	≤2.0ns	30pF	500Ω	open	2×V_{CC}	GND
2.7V	2.7V	≤2.5ns	50pF	500Ω	open	2×V_{CC}	GND
3.0V to 3.6V	2.7V	≤2.5ns	50pF	500Ω	open	2×V_{CC}	GND

4.3、AC Testing Waveforms



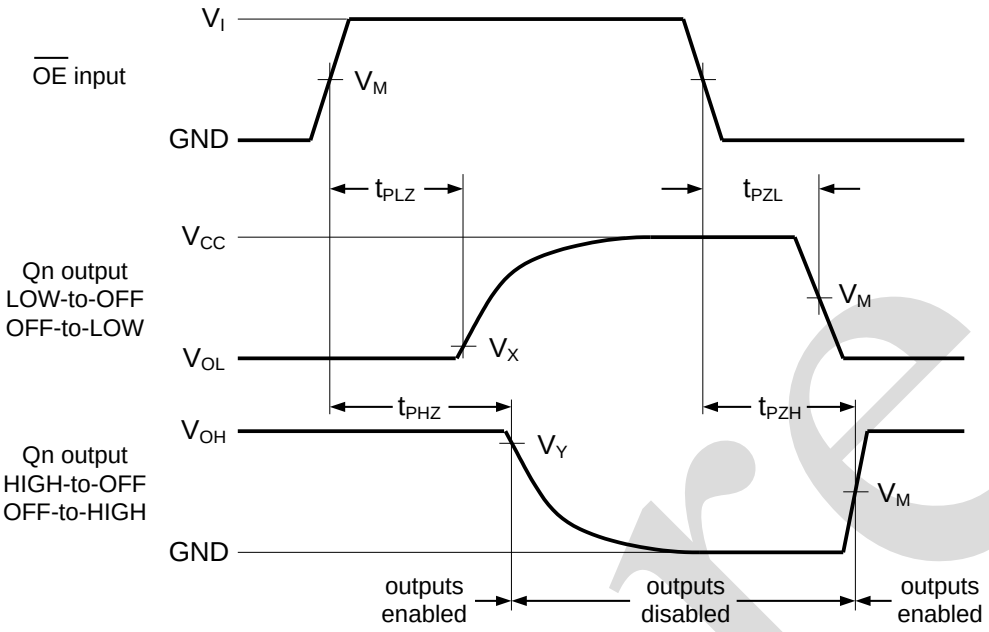
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. Input (Dn) to output (Qn) propagation delays



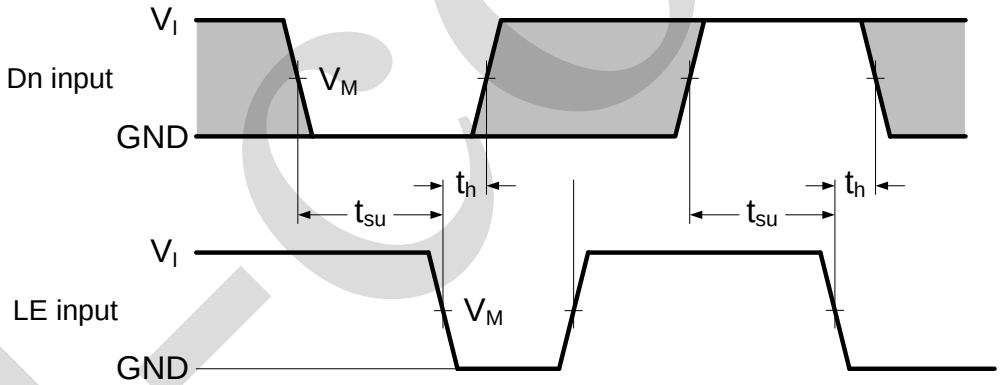
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. Latch Enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 8. 3-state enable and disable times



The shaded areas indicate when the input is permitted to change for predictable output performance.

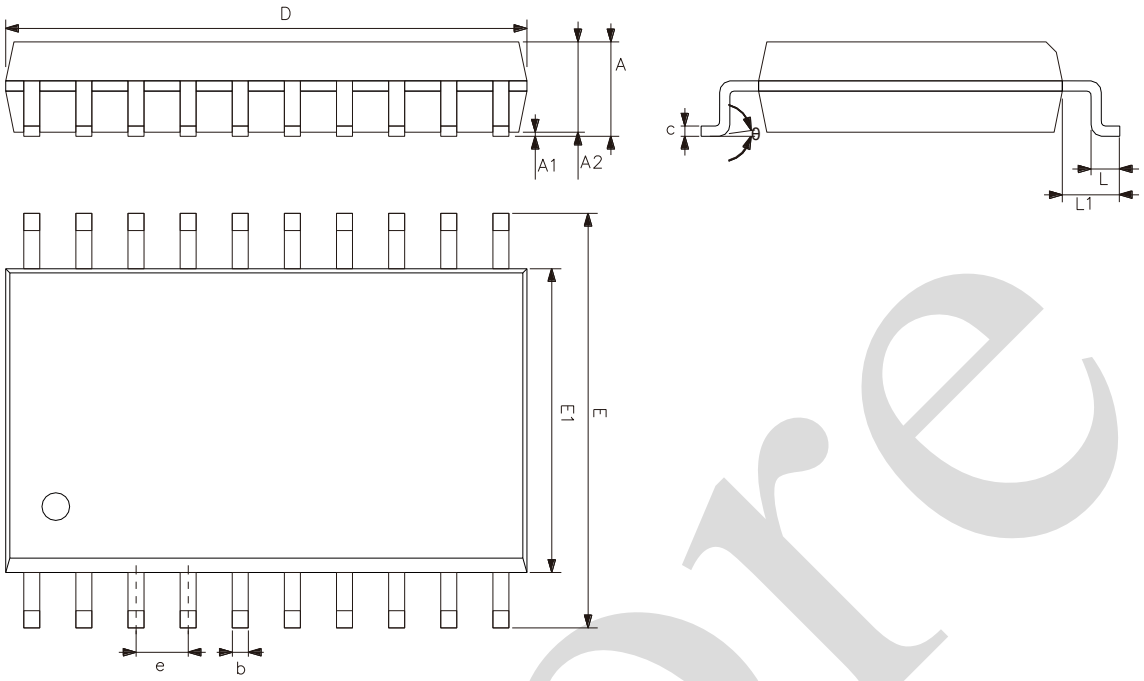
Figure 9. Data set-up and hold times for the Dn input to the LE input

4.4、Measurement Points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2V	V_{CC}	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
1.65V to 1.95V	V_{CC}	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
2.3V to 2.7V	V_{CC}	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
2.7V	2.7V	1.5V	1.5V	V_{OL}+0.3V	V_{OH}-0.3V
3.0V to 3.6V	2.7V	1.5V	1.5V	V_{OL}+0.3V	V_{OH}-0.3V

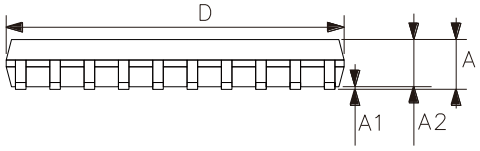
5、Package Information

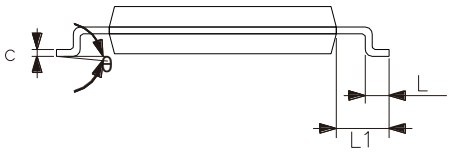
5.1、SOP20

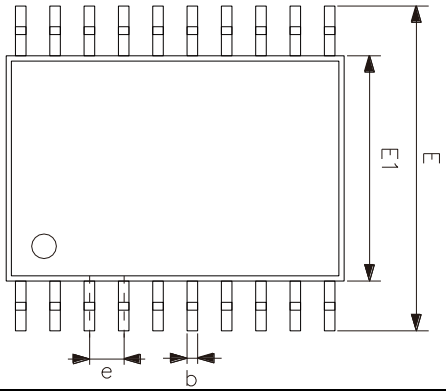


Symbol	Dimensions (mm)	
	Min.	Max.
A	2.47	2.65
A1	0.05	0.30
A2	2.20	2.44
b	0.35	0.50
c	0.15	0.30
D	12.54	12.94
E	10.00	10.60
E1	7.30	7.70
e	1.27	
L	0.40	1.05
L1	1.30	1.50
θ	0 °	8 °

5.2、TSSOP20

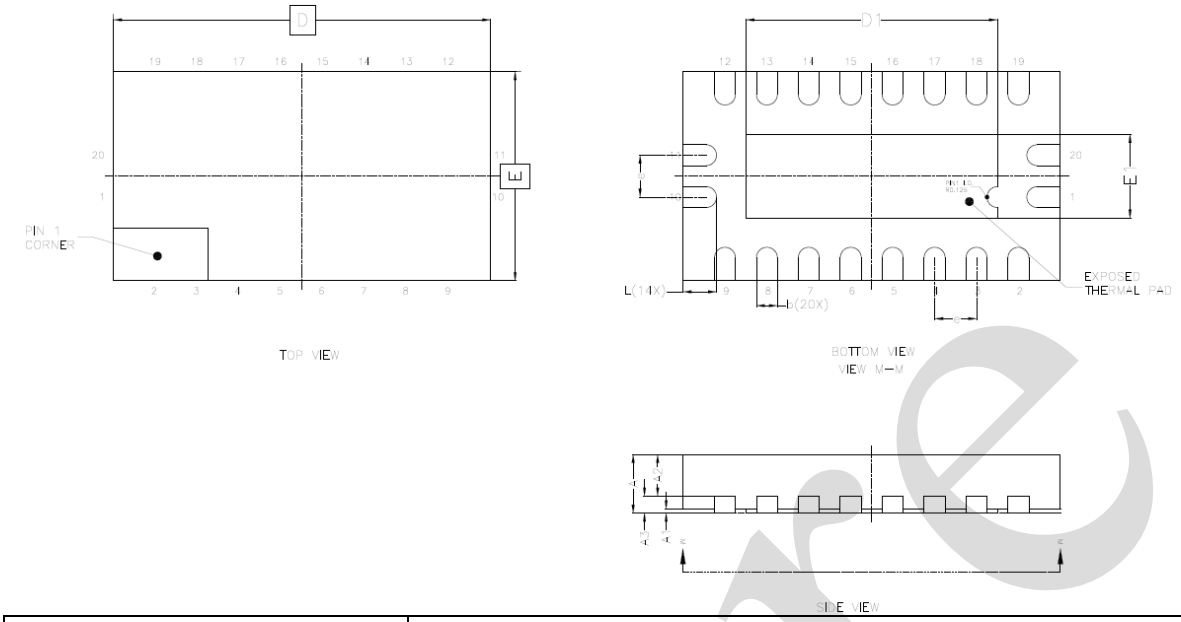






Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

5.3、DHVQFN20



Symbol	Dimensions (mm)	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.70
A3	0.20	
D	4.40	4.60
E	2.40	2.60
e	0.50	
b	0.18	0.30
L	0.30	0.50
D1	2.70	3.15
E1	0.70	1.15

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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